RELIABILITY REPORT

FOR

MAX4326ExA

PLASTIC ENCAPSULATED DEVICES

July 18, 2006

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR. SUNNYVALE, CA 94086

Written by

Jim Pedicord Quality Assurance Reliability Lab Manager

Conclusion

The MAX4326 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX4326 operational amplifier combines wide bandwidth and excellent DC accuracy with Rail-to-Rail operation at the inputs and outputs. This device consumes only $650\mu\text{A}$ per amplifier and operate from either a single supply (2.4V to 6.5V) or dual supplies ($\pm 1.2\text{V}$ to $\pm 3.25\text{V}$). This unity-gain-stable amplifier is capable of driving 250Ω loads and have a 5MHz gain-bandwidth product.

With their rail-to-rail input common-mode range and output swing, these amplifiers are ideal for low-voltage, single-supply operation. In addition, low offset voltage and high speed make them the ideal signal-conditioning stages for precision, low-voltage data-acquisition systems.

B. Absolute Maximum Ratings

<u>Item</u>	Rating		
Supply Voltage (VCC - VEE)	7.5V		
All Other Pins	(VCC + 0.3V) to (VEE - 0.3V)		
Output Short-Circuit Duration Continuous Power Dissipation (TA = +70°C)	Continuous (Short to Either Supply)		
8-Pin SO (derate 5.88mW/°C above +70°C)	471mW		
8-Pin µMAX (derate 4.10mW/°C above +70°C)	330mW		
Operating Temperature Range	-40°C to +85°C		
Maximum Junction Temperature	+150°C		
Storage Temperature Range	-65°C to +160°C		
Bump Reflow Temperature	+235°C		
Lead Temperature (soldering, 10s)	+300°C		

II. Manufacturing Information

A. Description: Low-Cost, +3V/+5V, 620µA, 200MHz, Single-Supply Op Amps with Rail-to-Rail Outputs

B. Process: CB30

C. Number of Device Transistors: 340

D. Fabrication Location: Oregon, USA

E. Assembly Location: Malaysia, Philippines or Thailand

F. Date of Initial Production: May, 1998

III. Packaging Information

A. Package Type: 8-Pin uMax 8-Pin SO

B. Lead Frame: Copper Copper

C. Lead Finish: Solder Plate or 100% Matte Tin Solder Plate or 100% Matte Tin

D. Die Attach: Silver-filled Epoxy Silver-filled Epoxy

E. Bondwire: Gold (1.0 mil dia.) Gold (1.0 mil dia.)

F. Mold Material: Epoxy with silica filler Epoxy with silica filler

G. Assembly Diagram: #05-0601-0523 #05-0601-0522

H. Flammability Rating: Class UL94-V0 Class UL94-V0

I. Classification of Moisture Sensitivity

per JEDEC standard J-STD-020-C: Level 1 Level 1

V. Die Information

A. Dimensions: 53 x 66 mils

B. Passivation: Si₃N₄/SiO₂ (Silicon nitride/ Silicon dioxide)

C. Interconnect: Gold

D. Backside Metallization: None

E. Minimum Metal Width: Metal 1: 1.4 microns Metal 2: 1.4 microns Metal 3: 3 microns (as drawn)

F. Minimum Metal Spacing: Metal 1: 1.6 microns Metal 2: 1.6 microns Metal 3: 3 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO₂

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Lab)

Bryan Preeshl (Managing Director of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 400 \times 2}$$
(Chi square value for MTTF upper limit)
$$\frac{1}{192 \times 4340 \times 400 \times 2}$$
Temperature Acceleration factor assuming an activation energy of 0.8eV
$$\lambda = 2.75 \times 10^{-9}$$

$$\lambda = 2.75 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5025) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1N**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The OA76-3 die type has been found to have all pins able to withstand a transient pulse of $\pm 2500V$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ± 250 mA.

Table 1 Reliability Evaluation Test Results

MAX4326ExA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Tes	t (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		400	0
Moisture Testi	ng (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	Umax NSO	77 77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	
Mechanical St	ress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots. Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/2/

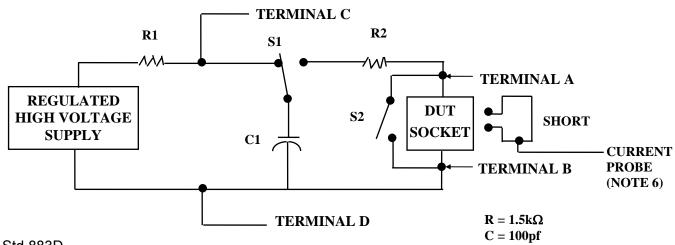
	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V _{PS1} 3/	All V _{PS1} pins
2.	All input and output pins	All other input-output pins

- 1/ Table II is restated in narrative form in 3.4 below.
- No connects are not to be tested.
 Repeat pin combination I for each named Power supply and for ground

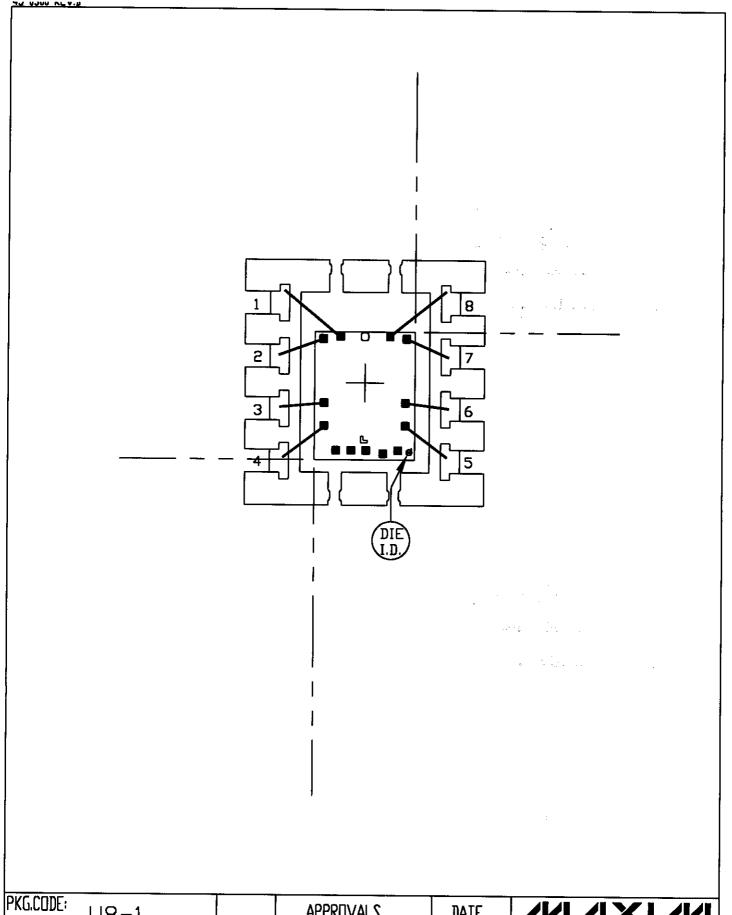
(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{RFF} , etc.).

3.4 Pin combinations to be tested.

- Each pin individually connected to terminal A with respect to the device ground pin(s) connected a. to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- Each pin individually connected to terminal A with respect to each different set of a combination b. of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- Each input and each output individually connected to terminal A with respect to a combination of C. all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D Method 3015.7 Notice 8



PKG.CODE: U8-1 APPROVALS DATE

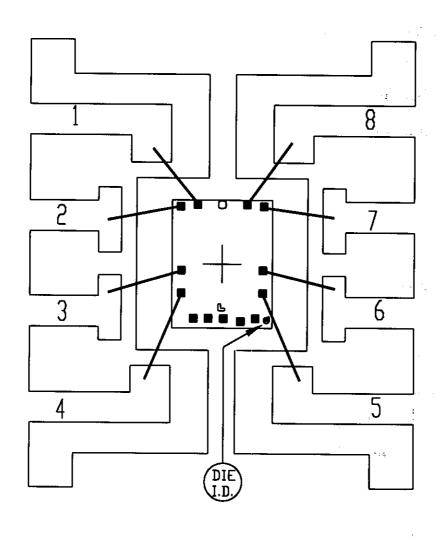
CAV./PAD SIZE: PKG.

68X94 DESIGN

APPROVALS

DATE

BUIL DSHEET NUMBER: REV.: 05-0601-0523 B



bkg'code: 28-5		APPROVALS	DATE	NIXIXI	//
CAV./PAD SIZE: 90 X 90	PKG. Design		- -	BUILDSHEET NUMBER: 05-0601-0522	REV.: B

