MAX4312ExE Rev. A

RELIABILITY REPORT

FOR

MAX4312ExE

PLASTIC ENCAPSULATED DEVICES

December 29, 2003

MAXIM INTEGRATED PRODUCTS

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Written by

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in

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Conclusion

The MAX4312 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX4312 single-supply mux-amp combines high-speed operation, low-glitch switching, and excellent video specifications. The MAX4312 is an integrated 8-channel multiplexer with an adjustable gain amplifier optimized for unity-gain stability. The device has 40ns channel switching time and low 10mVp-p switching transients, making it ideal for video-switching applications. It operates from a single +4V to +10.5V supply, or from dual supplies of $\pm 2V$ to $\pm 5.25V$, and it features Rail-to-Rail® outputs and an input common-mode voltage range that extends to the negative supply rail.

The MAX4312 has a -3dB bandwidth of 265MHz and up to a 460V/µs slew rate. Quiescent supply current is as low as 6.1mA, while low-power shutdown mode reduces supply current to as low as 560µA and places the outputs in a high-impedance state. The MAX4312's internal amplifier maintains an open-loop output impedance of only 8Ω over the full output voltage range, minimizing the gain error and bandwidth changes under loads typical of most rail-to-rail amplifiers. With differential gain and phase errors of 0.06% and 0.08°, respectively, this device is ideal for broadcast video applications.

B. Absolute Maximum Ratings

ltem	Rating
Supply Voltage (VCC to VEE)	12V
Input Voltage	(VEE - 0.3V) to (VCC + 0.3V)
All Other Pins	(VEE - 0.3V) to (VCC + 0.3V)
Output Current	±120mA
Short-Circuit Duration (VOUT to GND, VCC or VEE)	Continuous
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
16-Pin NSO	696mW
16-Pin QSOP	667mW
Derates above +70°C	
16-Pin SO	8.7mW/°C
16-Pin NQSOP	8.3mW/°C

II. Manufacturing Information

A. Description/Function:	High-Speed, Low-Power, Single-Supply Multichannel, Video Multiplexer-Ampl	lifier
B. Process:	CB2 - Complementary Bipolar Process	
C. Number of Device Transistor	156	
D. Fabrication Location:	Oregon, USA	
E. Assembly Location:	Philippines, Malaysia, Thailand or Korea	
F. Date of Initial Production:	July, 1997	

III. Packaging Information

A. Package Type:	16-Lead Small Outline	16-Lead QSOP
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-3001-0169	# 05-3001-0170
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1

IV. Die Information

A. Dimensions:	58 x 89 mils
B. Passivation:	Si ₃ N ₄ (Silicon nitride)
C. Interconnect:	Gold
D. Backside Metallization:	None
E. Minimum Metal Width:	2 microns (as drawn)
F. Minimum Metal Spacing:	2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

Α.	Quality Assurance Contacts:	Jim Pedicord (Manager, Rel Operations)
		Bryan Preeshl (Executive Director of QA)
		Kenneth Huening (Vice President)

- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
 0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \underbrace{1}_{\text{MTTF}} = \underbrace{1.83}_{192 \text{ x } 4389 \text{ x } 160 \text{ x } 2} \text{ (Chi square value for MTTF upper limit)}_{\text{Temperature Acceleration factor assuming an activation energy of 0.8eV}$$

$$\lambda = 6.79 \text{ x } 10^{-9}$$
 $\lambda = 6.79 \text{ F.I.T.}$ (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5276) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The OP53 die type has been found to have all pins able to withstand a transient pulse of ± 2500 V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ± 250 mA.

Table 1 Reliability Evaluation Test Results

MAX4312ExE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test	(Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		160	0
Moisture Testin	g (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SO QSOP	77 77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stre	ess (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots. Note 2: Generic Package/Process data

Attachment #1

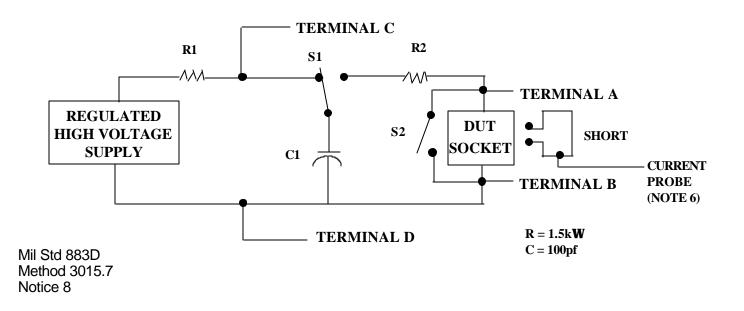
	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V _{PS1} <u>3/</u>	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

TABLE II. Pin combination to be tested. 1/2/

- 1/ Table II is restated in narrative form in 3.4 below.
- $\overline{2/}$ No connects are not to be tested.
- $\overline{3/}$ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, + V_{S} , - V_{S} , V_{REF} , etc).

- 3.4 <u>Pin combinations to be tested.</u>
 - a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
 - b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
 - c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



PKG.CODE; E16-1 APPROVALS DATE ////////////////////////////////////

