RELIABILITY REPORT

FOR MAX4271ESA+

PLASTIC ENCAPSULATED DEVICES

April 28, 2010

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

| **Approved by** |
|---|
| Richard Aburano |
| Quality Assurance |
| Manager, Reliability Operations |

**Conclusion**

The MAX4271ESA+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

**Table of Contents**



**I. Device Description**

A. General

The MAX4271/MAX4272/MAX4273 comprise a complete family of integrated 3V to 12V hot-swap controllers. They allow the safe insertion and removal of circuit cards into live backplanes. The discharged filter capacitors of the circuit card provide a low impedance to the live backplane. High in-rush currents from the backplane to the circuit card can burn up connectors and components, or momentarily collapse the backplane power supply leading to a system reset. This family of hot-swap controllers prevents such problems by regulating the current to a preset limit when the board is plugged in, allowing the system to stabilize safely. After the startup cycle is completed, two on-chip comparators provide DualSpeed/BiLevel(tm) protection against short circuits, load glitches, and overcurrent conditions. In the event of a fault condition, the load is disconnected. Fault recovery is handled by unlatching (MAX4271), autoretry (MAX4272), or programmed (MAX4273) methods. The MAX4271 family includes many integrated features that reduce component count and design time. An on-board charge pump provides the gate drive for a low-cost, external n-FET. Integrated features like startup current regulation and current glitch protection eliminate external timing resistors and capacitors. Also featured are an open-drain status output to indicate a fault condition, and an adjustable overcurrent response time. The MAX4271 (latched fault protection) and MAX4272 (autoretry fault protection) come in 8-pin SO packages. The MAX4273 (full function) comes in the space-saving 16-pin QSOP package and 16-pin SO package. All parts are specified across the extended temperature range, and have an absolute maximum rating of 15V to provide extra protection against inductive kickback during board removal.

## II. Manufacturing Information

| | |
|---|---|
| A. Description/Function: | 3V to 12V, Current-Limiting, Hot Swap Controllers with Autoretry, DualSpeed/BiLevel Fault Protection |
| B. Process: | S3 |
| C. Number of Device Transistors: | |
| D. Fabrication Location: | Oregon |
| E. Assembly Location: | Malaysia, Philippines, Thailand |
| F. Date of Initial Production: | April 22, 2000 |

## III. Packaging Information

| | |
|---|---|
| A. Package Type: | 8-pin SOIC (N) |
| B. Lead Frame: | Copper |
| C. Lead Finish: | 100% matte Tin |
| D. Die Attach: | Conductive |
| E. Bondwire: | Au (1 mil dia.) |
| F. Mold Material: | Epoxy with silica filler |
| G. Assembly Diagram: | #05-3001-0172 |
| H. Flammability Rating: | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C | Level 1 |
| J. Single Layer Theta Ja: | 170°C/W |
| K. Single Layer Theta Jc: | 40°C/W |
| L. Multi Layer Theta Ja: | 128.4°C/W |
| M. Multi Layer Theta Jc: | 36°C/W |

## IV. Die Information

| | |
|---|---|
| A. Dimensions: | 87 X 145 mils |
| B. Passivation: | $Si_3N_4/SiO_2$ (Silicon nitride/ Silicon dioxide) |
| C. Interconnect: | Al/0.5%Cu with Ti/TiN Barrier |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | 3.0 microns (as drawn) |
| F. Minimum Metal Spacing: | 3.0 microns (as drawn) |
| G. Bondpad Dimensions: | 5 mil. Sq. |
| H. Isolation Dielectric: | $SiO_2$ |
| I. Die Separation Method: | Wafer Saw |

## V. Quality Assurance Information

| | |
|---|---|
| A. Quality Assurance Contacts: | Richard Aburano (Manager, Reliability Operations)<br>Bryan Preeshl (Managing Director of QA) |
| B. Outgoing Inspection Level: | 0.1% for all electrical parameters guaranteed by the Datasheet.<br>0.1% For all Visual Defects. |
| C. Observed Outgoing Defect Rate: | < 50 ppm |
| D. Sampling Plan: | Mil-Std-105D |

## VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ($\lambda$) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{6.21}{192 \times 4340 \times 160 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 23.3 \times 10^{-9}$

$\lambda = 23.3$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the S3 Process results in a FIT Rate of 0.04 @ 25C and 0.69 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The OP00 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2500V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of 250mA.

**Table 1**
Reliability Evaluation Test Results

**MAX4271ESA+**

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | SAMPLE SIZE | NUMBER OF FAILURES |
|---|---|---|---|---|
| **Static Life Test** (Note 1) | | | | |
| | Ta = 135°C<br>Biased<br>Time = 192 hrs. | DC Parameters & functionality | 160 | 2 |
| **Moisture Testing** (Note 2) | | | | |
| HAST | Ta = 130°C<br>RH = 85%<br>Biased<br>Time = 96hrs. | DC Parameters & functionality | 135 | 0 |
| **Mechanical Stress** (Note 2) | | | | |
| Temperature Cycle | -65°C/150°C<br>1000 Cycles<br>Method 1010 | DC Parameters & functionality | 153 | 0 |

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data