RELIABILITY REPORT

FOR

MAX4234ASD+ / MAX4234AUD+

PLASTIC ENCAPSULATED DEVICES

February 24, 2011

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

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Approved by
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Quality Assurance
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Conclusion

The MAX4234ASD+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX4230-MAX4234 single/dual/quad, high-output-drive CMOS op amps feature 200mA of peak output current, rail-to-rail input, and output capability from single 2.7V to 5.5V supply. These amplifiers exhibit high slew rate of 10V/µs and a gain-bandwidth product (GBWP) of 10MHz. The MAX4230-MAX4234 can drive typical headset levels (32), as well as bias an RF power amplifier (PA) in wireless handset applications. The MAX4230 comes in a tiny 5-pin SC70 package and the MAX4231, single with shutdown, is offered in a 6-pin SC70 package and in 1.5mm x 1.0mm UCSP(tm) and thin µDFN packages. The dual op-amp MAX4233 offered in the space-saving 10-bump chip-scale package (UCSP), providing the smallest footprint area for a dual op amp with shutdown. These op amps are designed to be part of the PA control circuitry, biasing RF PAs in wireless headsets. The MAX4231/MAX4233 offer a active-low SHDN feature that drives the output low. This ensures that the RF PA is fully disabled when needed, preventing unconverted signals to the RF antenna. The MAX4230 family offers low offsets, wide bandwidth, and high-output drive in a tiny 2.1mm x 2.0mm space-saving SC70 package. These parts are offered over the automotive temperature range (-40°C to +125°C).

II. Manufacturing Information

A. Description/Function:	High-Output-Drive, 10MHz, 10V/µs, Rail-to-Rail I/O Op Amps with Shutdown in SC70
B. Process:	TS50
C. Number of Device Transistors:	
D. Fabrication Location:	Taiwan
E. Assembly Location:	Malaysia, Philippines, Thailand
F. Date of Initial Production:	January 26, 2002

III. Packaging Information

A. Package Type:	14-pin SOIC (N)	14-pin TSSOP
B. Lead Frame:	Copper	Copper
C. Lead Finish:	100% matte Tin	100% matte Tin
D. Die Attach:	Conductive	Conductive
E. Bondwire:	Au (1 mil dia.)	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-0294	#05-9000-3639
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1	Level 1
J. Single Layer Theta Ja:	120°C/W	110°C/W
K. Single Layer Theta Jc:	37°C/W	30°C/W
L. Multi Layer Theta Ja:	N/A	100.4°C/W
M. Multi Layer Theta Jc:	N/A	30°C/W

IV. Die Information

A. Dimensions:	56 X 56 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.50µm
F. Minimum Metal Spacing:	0.50µm
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{700 \times 4340 \times 118 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 2.6 \times 10^{-9}$

λ = 2.6 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the TS50 Process results in a FIT Rate of 0.25 @ 25C and 6.11 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (ESD lot K9L0BQ001R D/C 0819, Latch-Up lot K9L0BQ003B D/C 0509)

The OX79 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX4234ASD+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C	DC Parameters	39	0	K9L0BQ001R, D/C 0819
	Biased	& functionality	79	0	K9L0BQ002C, D/C 0845
	Time = 700 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots.