

RELIABILITY REPORT
FOR
MAX4233ABC+T
CHIP SCALE PACKAGE

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MAXIM INTEGRATED

160 RIO ROBLES
SAN JOSE, CA 95134

Approved by
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Conclusion

The MAX4233ABC+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I.Device Description	IV.Die Information
II.Manufacturing Information	V.Quality Assurance Information
III.Packaging Information	VI.Reliability Evaluation
.....Attachments	

I. Device Description

A. General

The MAX4230-MAX4234 single/dual/quad, high-output-drive CMOS op amps feature 200mA of peak output current, rail-to-rail input, and output capability from single 2.7V to 5.5V supply. These amplifiers exhibit high slew rate of 10V/μs and a gain-bandwidth product (GBWP) of 10MHz. The MAX4230-MAX4234 can drive typical headset levels (32), as well as bias an RF power amplifier (PA) in wireless handset applications. The MAX4230 comes in a tiny 5-pin SC70 package and the MAX4231, single with shutdown, is offered in a 6-pin SC70 package and in 1.5mm x 1.0mm UCSP(tm) and thin μDFN packages. The dual op-amp MAX4233 offered in the space-saving 10-bump chip-scale package (UCSP), providing the smallest footprint area for a dual op amp with shutdown. These op amps are designed to be part of the PA control circuitry, biasing RF PAs in wireless headsets. The MAX4231/MAX4233 offer a active-low SHDN feature that drives the output low. This ensures that the RF PA is fully disabled when needed, preventing unconverted signals to the RF antenna. The MAX4230 family offers low offsets, wide bandwidth, and high-output drive in a tiny 2.1mm x 2.0mm space-saving SC70 package. These parts are offered over the automotive temperature range (-40°C to +125°C).

II. Manufacturing Information

A. Description/Function:	High-Output-Drive, 10MHz, 10V/ μ s, Rail-to-Rail I/O Op Amps with Shutdown in SC70
B. Process:	VS50
C. Number of Device Transistors:	
D. Fabrication Location:	Taiwan
E. Assembly Location:	Texas or Philippines
F. Date of Initial Production:	October 27, 2001

III. Packaging Information

A. Package Type:	12-pin UCSP
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	N/A
E. Bondwire:	N/A
F. Mold Material:	N/A
G. Assembly Diagram:	#05-9000-3928
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	N/A
K. Single Layer Theta Jc:	N/A
L. Multi Layer Theta Ja:	N/A
M. Multi Layer Theta Jc:	N/A

IV. Die Information

A. Dimensions:	83 X 63 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.50 μ m
F. Minimum Metal Spacing:	0.50 μ m
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

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|-----------------------------------|--|
| A. Quality Assurance Contacts: | Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA) |
| B. Outgoing Inspection Level: | 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects. |
| C. Observed Outgoing Defect Rate: | < 50 ppm |
| D. Sampling Plan: | Mil-Std-105D |

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{500 \times 4340 \times 45 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 9.4 \times 10^{-9}$$

$$\lambda = 9.4 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the VS50 Process results in a FIT Rate of 0.3 @ 25C and 5.07 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (lot KKF0AQ001, D/C 0209)

The OX78 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX4233ABC+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 500 hrs.	DC Parameters & functionality	45	0	KKF0CA007A, D/C 0209

Note 1: Life Test Data may represent plastic DIP qualification lots.