### RELIABILITY REPORT

FOR

# **MAX4137EWG**

PLASTIC ENCAPSULATED DEVICES

April 6, 2004

# **MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

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#### Conclusion

The MAX4137 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX4137 are 1-input/4-output voltage-feedback amplifiers that combine high speed with fast switching for video distribution applications. The MAX4137 is internally set for a closed-loop gain of 2V/V.

The MAX4137 achieves a -3dB bandwidth of 185MHz, with 0.1dB gain flatness to 40MHz. The device delivers a 1000V/µs slew rate, as well as exceptional full-power bandwidths of 185MHz.

A 25ns channel switching time enables rapid multiplexing for picture-in-picture applications, yet maintains a high off-isolation of 75dB and all-hostile crosstalk of -50dB (f = 30MHz). The MAX4137's on-board logic selects any combination of the four signal outputs. Each output is capable of swinging ±2V and delivering up to 65mA of current.

Rating

### B. Absolute Maximum Ratings

Item

<del>o</del>	<u>rtaming</u>
Power-Supply Voltage (VCC to VEE)	12V
Voltage on Any Input Pin to GND	(VCC + 0.3V) to $(VEE - 0.3V)$
Short-Circuit Duration to GND	Continuous
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +160°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
24-Pin WSO	1540mW
Derates above +70°C	
24-Pin WSO	19.3mW/°C

# II. Manufacturing Information

A. Description/Function: 350MHz, Ultra-Low-Noise Op Amp

B. Process: CP10 (Recessed-Oxide-Isolated, High Speed Complementary Bipolar Process)

C. Number of Device Transistors: 625

D. Fabrication Location: Oregon, USA

E. Assembly Location: Malaysia

F. Date of Initial Production: September, 1996

### III. Packaging Information

A. Package Type: 24- Lead WSO

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: Silver-filled Epoxy

E. Bondwire: Gold (1.3 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: Buildsheet # 05-0601-0485

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity

per JEDEC standard J-STD-020-A: Level 1

### IV. Die Information

A. Dimensions: 91 x 109 mils

B. Passivation: SiN/SiO (nitride/oxide)

C. Interconnect: Aluminum/Si (Si = 1%)

D. Backside Metallization: None

E. Minimum Metal Width: 2 microns (as drawn)

F. Minimum Metal Spacing: 2 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO<sub>2</sub>

I. Die Separation Method: Wafer Saw

### V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)

Bryan Preeshl (Executive Director)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

### VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \underbrace{\frac{1}{\text{MTTF}}}_{} = \underbrace{\frac{1.83}{192 \times 4389 \times 80 \times 2}}_{} \text{(Chi square value for MTTF upper limit)}$$

$$\underbrace{\text{Temperature Acceleration factor assuming an activation energy of } 0.8eV$$

$$\lambda = 13.57 \times 10^{-9}$$

 $\lambda$  = 13.57 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5211) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (RR-1M).

#### B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

### C. E.S.D. and Latch-Up Testing

The OA89 die type has been found to have all pins able to withstand a transient pulse of  $\pm 2000$ V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 100$ mA.

# Table 1 Reliability Evaluation Test Results

# MAX4137EWG

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test	t (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
Moisture Testii	ng (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	WSO	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Str	ress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots. Note 2: Generic Package/Process data

#### Attachment #1

TABLE II. Pin combination to be tested. 1/2/

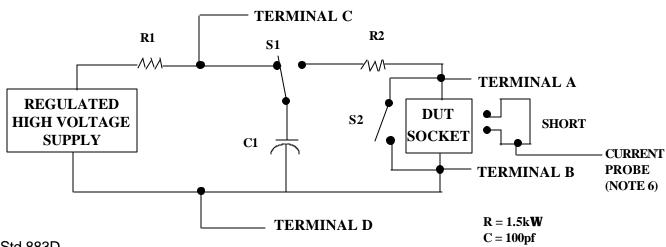
	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V <sub>PS1</sub> 3/	All V <sub>PS1</sub> pins
2.	All input and output pins	All other input-output pins

- 1/ Table II is restated in narrative form in 3.4 below.
- 2/ No connects are not to be tested.
- 3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ , GND,  $+V_{S.}$  - $V_{S.}$ ,  $V_{REF}$ , etc).

# 3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., \( \lambda\_{S1} \), or \( \lambda\_{S2} \) or \( \lambda\_{S3} \) or \( \lambda\_{CC1} \), or \( \lambda\_{CC2} \)) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D Method 3015.7 Notice 8

