RELIABILITY REPORT

FOR

MAX4027ESD+

PLASTIC ENCAPSULATED DEVICES

December 4, 2015

**MAXIM INTEGRATED**

160 RIO ROBLES

SAN JOSE, CA 95134

| **Approved by** |
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| Sokhom Chum |
| Quality Assurance |
| Reliability Engineer |

## Conclusion

The MAX4027ESD+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

## Table of Contents



## I. Device Description

A. General

The MAX4027 is a triple, wideband, 2-channel, noninverting gain-of-two video amplifier with input multiplexing, capable of driving up to two back-terminated video loads. The MAX4027 features current-mode feedback amplifiers configured for a gain of two (+6dB) with a -3dB large-signal bandwidth of 200MHz. The device has low (0.012%/0.014°) differential gain and phase errors, and operates from ±5V supplies. The MAX4027 is ideal for use in broadcast and graphics video systems because of the low 2pF input capacitance, channel-to-channel switching time of only 15ns, and wide 62MHz, large-signal 0.1dB bandwidth. High-impedance output disabling allows the MAX4027 to be incorporated into large switching arrays with minimal interaction with the source. Specified over the -40°C to +85°C extended temperature range, the MAX4027 is available in 14-pin SO and TSSOP packages.

## II. Manufacturing Information

| | |
|---|---|
| A. Description/Function: | 225MHz, Triple, 2-Channel Video Multiplexer-Amplifier |
| B. Process: | CB2 |
| C. Number of Device Transistors: | |
| D. Fabrication Location: | Oregon |
| E. Assembly Location: | Philippines, Thailand |
| F. Date of Initial Production: | October 02, 2003 |

## III. Packaging Information

| | |
|---|---|
| A. Package Type: | 14-pin SOIC (N) |
| B. Lead Frame: | Copper |
| C. Lead Finish: | 100% matte Tin |
| D. Die Attach: | Conductive |
| E. Bondwire: | Au (1 mil dia.) |
| F. Mold Material: | Epoxy with silica filler |
| G. Assembly Diagram: | #05-9000-0719 |
| H. Flammability Rating: | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C | Level 1 |
| J. Single Layer Theta Ja: | 120°C/W |
| K. Single Layer Theta Jc: | 37°C/W |
| L. Multi Layer Theta Ja: | 84°C/W |
| M. Multi Layer Theta Jc: | 34°C/W |

## IV. Die Information

| | |
|---|---|
| A. Dimensions: | 72X135 mils |
| B. Passivation: | $Si_3N_4$ (Silicon nitride) |
| C. Interconnect: | Au |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | 2 microns (as drawn) |
| F. Minimum Metal Spacing: | 2 microns (as drawn) |
| G. Bondpad Dimensions: | |
| H. Isolation Dielectric: | $SiO_2$ |
| I. Die Separation Method: | Wafer Saw |

## V. Quality Assurance Information

| | |
|---|---|
| A. Quality Assurance Contacts: | Don Lipps (Manager, Reliability Engineering)<br>Bryan Preeshl (Vice President of QA) |
| B. Outgoing Inspection Level: | 0.1% for all electrical parameters guaranteed by the Datasheet.<br>0.1% for all Visual Defects. |
| C. Observed Outgoing Defect Rate: | < 50 ppm |
| D. Sampling Plan: | Mil-Std-105D |

## VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ($\lambda$) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 9706 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 9706 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 10.2 \times 10^{-9}$

$\lambda = 10.2$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the CB2 Process results in a FIT Rate of 0.06 @ 25C and 0.95 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot NGV0AQ001C, 0330)

The VA24 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

**Table 1**

Reliability Evaluation Test Results

**MAX4027ESD+**

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | SAMPLE SIZE | NUMBER OF FAILURES | COMMENTS |
|---|---|---|---|---|---|
| **Static Life Test** (Note 1) | Ta = 150°C<br>Biased<br>Time = 192 hrs. | DC Parameters & functionality | 48 | 0 | NGV0AQ001C, D/C 0330 |

Note 1: Life Test Data may represent plastic DIP qualification lots.