RELIABILITY REPORT

FOR

MAX40008ANT+T

WAFER LEVEL DEVICES

August 3, 2017

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

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Conclusion

The MAX40008ANT+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX40008/MAX40009 are single micropower comparators featuring low-voltage operation and rail-to-rail inputs. Their operating supply voltage range from 1.7V to 5.5V, which makes them ideal for systems running from nominal 1.8V to 5V supplies. While only consuming 12µA of supply current, the MAX40008/MAX40009 achieve a 220ns propagation delay. These devices feature 0.5mV (typ) input offset voltage and internal hysteresis, ensuring clean output switching, even with slow-moving input signals. The output stage’s unique design limits supply-current surges while switching, virtually eliminating the supply glitches typical of many other comparators. The MAX40009 has a push-pull output stage, while the MAX40008 has an open-drain output stage that can be pulled beyond VDD to 6V (max) above GND input. The open-drain version is ideal for level translators and bipolar to single-ended converters. The MAX40008/MAX40009 are available in tiny 0.73mm x 1.1mm 6-bump wafer-level packages (WLPs), significantly reducing the required board area. An alternative 6-pin SOT23 package is also available. These devices are fully specified over the -40°C to +125°C automotive temperature range.

II. Manufacturing Information

A. Description/Function:	220ns, 12µA, 6-Bump WLP Comparators with Shutdown
B. Process:	S18
C. Fabrication Location:	USA
D. Assembly Location:	Taiwan
E. Date of Initial Production:	June 8, 2017

III. Packaging Information

A. Package Type:	6-bump thin WLP
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	None
E. Bondwire:	N/A (N/A mil dia.)
F. Mold Material:	None
G. Assembly Diagram:	#05-100502
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	N/A°C/W
K. Single Layer Theta Jc:	N/A°C/W
L. Multi Layer Theta Ja:	98.06°C/W
M. Multi Layer Theta Jc:	N/A°C/W

IV. Die Information

A. Dimensions:	43.7008X29.9213 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Isolation Dielectric:	SiO_2
H. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Eric Wright (Reliability Engineering) Brian Standley (Manager, Reliability) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

λ = 13.7 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.40 @ 25C and 6.96 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The CC04 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX40008ANT+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.