RELIABILITY REPORT

FOR

MAX3991UTG+

PLASTIC ENCAPSULATED DEVICES

February 19, 2010

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
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Conclusion

The MAX3991UTG+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX3991 is a 10Gbps clock and data recovery (CDR) with limiting amplifier IC for XFP optical receivers. The MAX3991 and the MAX3992 (CDR with equalizer) form a signal conditioner chipset for use in XFP transceiver modules. The chipset is XFI compliant and offers multirate operation for data rates from 9.95Gbps to 11.1Gbps. The MAX3991 has 7mVP-P input sensitivity (BER 10-12), which allows direct connection to a transimpedance amplifier without the use of a stand-alone limiting amplifier. The phase-locked loop (PLL) is optimized for jitter tolerance and provides 0.6UI of high-frequency tolerance in SONET, Ethernet, and Fibre-Channel applications. The MAX3991 output provides 27% margin to the XFP eye mask specification. An AC-based power detector toggles the loss-of-signal (LOS) output when the input signal swing is below the user-programmed assert threshold. An external reference clock, with frequency equal to 1/64 or 1/16 of the serial data rate is used to aid in frequency acquisition. A loss-of-lock (LOL) indicator is provided to indicate the lock status of the receiver PLL. The MAX3991 is available in a 4mm x 4mm, 24-pin QFN package. It consumes 350mW from a single +3.3V supply and operates over the 0°C to +85°C temperature range.

II. Manufacturing Information

A. Description/Function:	10Gbps Clock and Data Recovery with Limiting Amplifier
B. Process:	F120
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon
E. Assembly Location:	China, Malaysia, Philippines, Thailand
F. Date of Initial Production:	October 23, 2004

III. Packaging Information

A. Package Type:	24-pin TQFN 4x4
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-1124
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	48°C/W
K. Single Layer Theta Jc:	2.7°C/W
L. Multi Layer Theta Ja:	36°C/W
M. Multi Layer Theta Jc:	2.7°C/W

IV. Die Information

A. Dimensions:	100 X 100 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Au with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn) Metal 1, 2 & 3 5.6 microns (as drawn) Metal 4
F. Minimum Metal Spacing:	1.6 microns (as drawn) Metal 1, 2 & 3, 4.2 microns (as drawn) Metal 4
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 50 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 9.83 \times 10^{-9}$

$\lambda = 9.83$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim"s reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the F120 Process results in a FIT Rate of 0.33 @ 25C and 5.73 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The HD45 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500 V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX3991UTG+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality	50	0
Moisture Testing (Note 2)				
HAST	Ta = 130°C RH = 85% Biased Time = 96hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data