MAX392ESE
Rev. A

RELIABILITY REPORT

FOR

MAX392ESE
MAX391 – MAX393

PLASTIC ENCAPSULATED DEVICES

December 5, 2008

MAXIM INTEGRATED PRODUCTS

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Conclusion

The MAX392 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX391/MAX392/MAX393 are precision, quad, single-pole/single-throw (SPST) analog switches designed to operate at +3V, +5V, or ±5V. The MAX391 has four normally closed (NC) switches, and the MAX392 has four normally open (NO) switches. The MAX393 has two NO and two NC switches. All three devices offer low leakage (100pA max) and fast switching speeds ($t_{ON} \leq 130ns$, $t_{OFF} \leq 75ns$). Power consumption is just 1µW—ideal for battery-operated equipment. All devices operate from a single +3V to +15V supply or from dual ±3.0V to ±8V supplies.

With ±5V supplies, the MAX391/MAX392/MAX393 offer guaranteed 2Ω max channel-to-channel matching, 30Ω max on-resistance (R_{ON}), and 4Ω max R_{ON} flatness over the specified range.

These switches are also fully specified for single +5V operation, with 2Ω max R_{ON} match, 60Ω max R_{ON}, and 6Ω max flatness.

These low-voltage switches also offer 5pC max charge injection, and ESD protection is greater than 2000V, per method 3015.7.

B. Absolute Maximum Ratings

Item	Rating
Voltage Referenced to VV+.	-0.3V to +17V
GND	-0.3V to +17V
GND	-0.3V to (V+ + 0.3V)
VIN, VCOM, VNC, VNO (Note 1)	V- to V+
Current (any terminal)	30mA
Peak Current, COM, NO, NC (pulsed at 1ms, 10% duty cycle max)	100mA
ESD per Method 3015.7	>2000V
Continuous Power Dissipation (TA = +70°C)	
Plastic DIP (derate 10.53mW/°C above+70°C)	842mW
Narrow SO (derate 8.70mW/°C above +70°C)	696mW
TSSOP (derate 6.7mW/°C above +70°C)	457mW
CERDIP (derate 10.00mW/°C above +70°C)	800mW
QFN (derate 18.5mW/°C above +70°C)	1481mW
Operating Temperature Ranges	
MAX39_C_ _	0°C to +70°C
MAX39_E_ _	-40°C to +85°C
MAX39_M_ _	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

II. Manufacturing Information

A. Description/Function:	**Precision, Quad, SPST Analog Switches**
B. Process:	SG5 - Standard 5 micron silicon gate CMOS
C. Number of Device Transistors:	76
D. Fabrication Location:	USA
E. Assembly Location:	Malaysia, Philippines, Thailand
F. Date of Initial Production:	February 1994

III. Packaging Information

A. Package Type:	16-Lead Wide SO
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate or 100% Matte Tin
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)
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F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-0301-0634
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1

IV. Die Information

A. Dimensions:	67 x 102 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	5 microns (as drawn)
F. Minimum Metal Spacing:	5 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Operations)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 559 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 1.97 \times 10^{-9}$

λ = 1.97 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the SG5 Process results in a FIT Rate of 0.4 @ 25C and 7.4 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The AG64 die type has been found to have all pins able to withstand a transient pulse of ±3000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX392ESE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		559	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	NSO	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.