MAX3890ECB
Rev. A

RELIABILITY REPORT

FOR

MAX3890ECB

PLASTIC ENCAPSULATED DEVICES

March 5, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

Jim Pedicord
Quality Assurance
Reliability Lab Manager

Reviewed by

Bryan J. Preeshl
Quality Assurance
Executive Director

Conclusion

The MAX3890 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX3890 serializer is ideal for converting 16-bit-wide, 155Mbps parallel data to 2.5Gbps serial data in ATM and SDH/SONET applications. Operating from a single +3.3V supply, this device accepts low-voltage differential-signal (LVDS) clock and data inputs for interfacing with high-speed digital circuitry, and delivers positive-referenced emitter-coupled logic (PECL) serial data and clock outputs. A fully integrated phase-locked loop (PLL) synthesizes an internal 2.5GHz serial clock from a 155.52MHz, 77.76MHz, 51.84MHz, or 38.88MHz reference clock. A loopback data output is provided to facilitate system diagnostic testing.

B. Absolute Maximum Ratings

Item	Rating
Terminal Voltage (with respect to GND)	
V_{CC}	-0.5V to +5V
All Inputs, FIL+, FIL-	-0.5V to (V_{CC} + 0.5V)
Output current	
LVDS Outputs (PCLKO±)	10mA
PECL Outputs (SDO±, SCLKO±)	50mA
CML Outputs (SLBO±)	15mA
Storage Temp.	-65°C to +150°C
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation (TA = +70°C)	
64-Pin TQFP	1000mW
Derates above +70°C	
64-Pin TQFP	44.8mW/°C

II. Manufacturing Information

A. Description/Function: +3.3V, 2.5Gbps, SDH/SONET 16:1 Serializer with Clock Synthesis and LVDS Inputs

B. Process: GST-2 (High Speed Double Poly-Silicon Bipolar Process)

C. Number of Device Transistors: 4,626

D. Fabrication Location: Oregon, USA

E. Assembly Location: Korea

F. Date of Initial Production: June, 1999

III. Packaging Information

A. Package Type: 64 Lead TQFP-EP (Thin Quad Flat Pack, Exposed Pad)

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: Silver-filled Epoxy

E. Bondwire: Gold (1.2 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: Buildsheet # 05-7001-0385

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1

IV. Die Information

A. Dimensions: 124 x 116 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Poly / Au

D. Backside Metallization: None

E. Minimum Metal Width: 1.4 microns (as drawn)

F. Minimum Metal Spacing: 1.4 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord	(Manager, Rel Operations)
Bryan Preeshl	(Executive Director of QA)
Kenneth Huening	(Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times \underbrace{9823}_{} \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 10.11 \times 10^{-9}$ $\lambda = 10.11$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The HF16 die type has been found to have all pins able to withstand a transient pulse of ±200V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing on all I/O Pins has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX3890ECB

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0
Moisture Testing				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic Package/Process data.

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

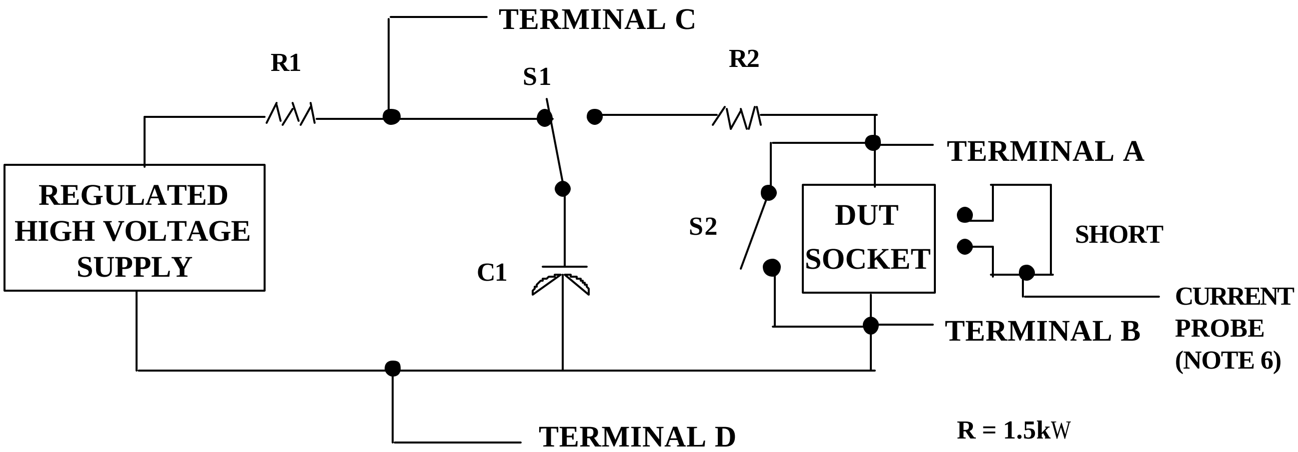
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_{S,}$ $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

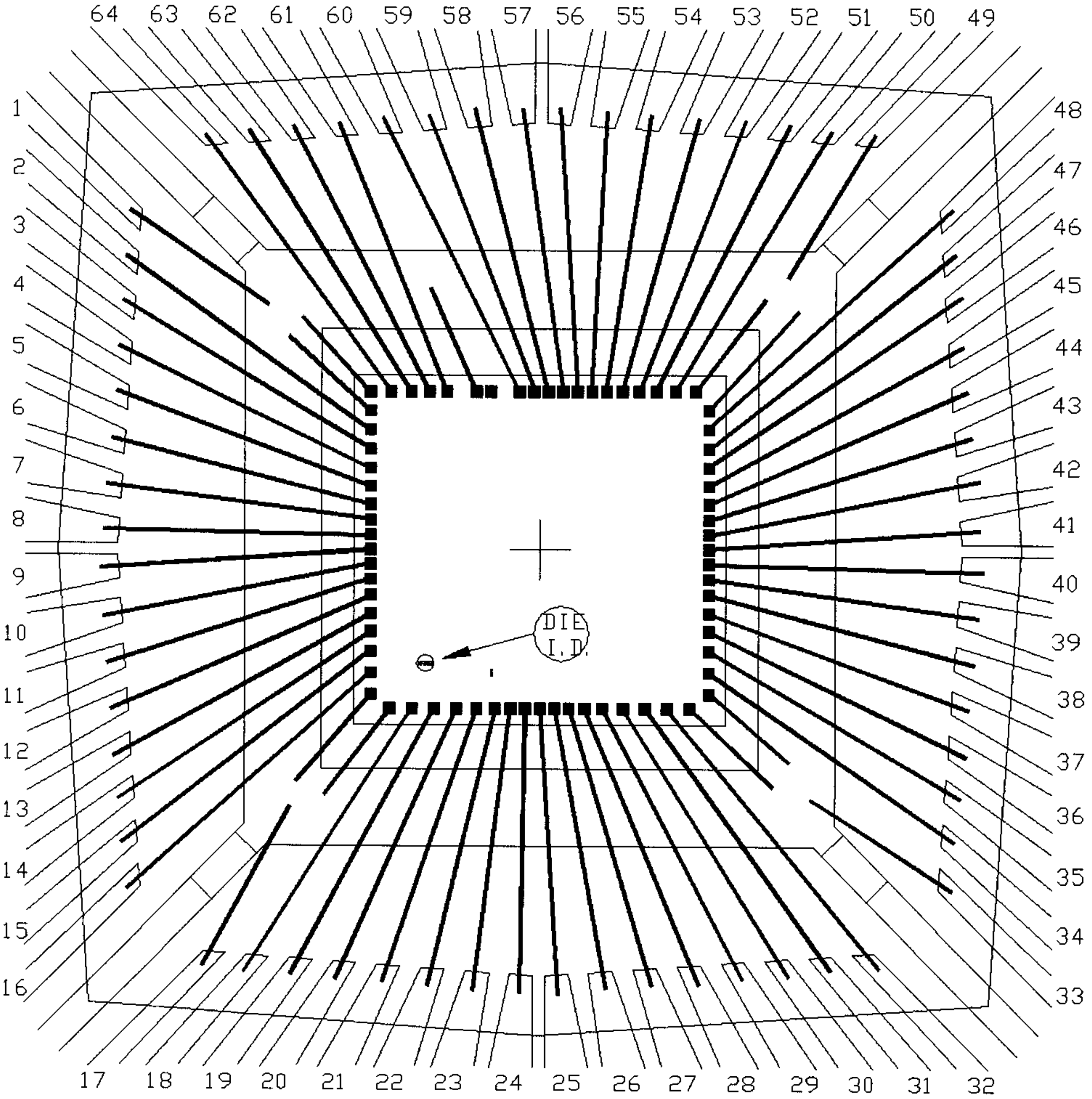
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



R = 1.5kΩ
C = 100pf



PKG. CODE: C64E-3		APPROVALS	DATE		
CAV./PAD SIZE: 197×197	PKG. DESIGN			BUILDSHEET NUMBER: 05-7001-0385	REV.: A