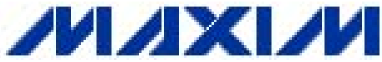

RELIABILITY REPORT

FOR

MAX3873AETP+

PLASTIC ENCAPSULATED DEVICES

September 22, 2010

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
Manager, Reliability Engineering

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Conclusion

The MAX3873AETP+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim''s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim''s quality and reliability standards.

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I. Device Description

A. General

The MAX3873A is a compact, low-power 2.488Gbps/2.67Gbps clock-recovery and data-retiming IC for SDH/SONET applications. The phase-locked loop (PLL) recovers a synchronous clock signal from the serial NRZ data input. The input data is then retimed by this recovered clock, providing a clean data output. The MAX3873A meets all SDH/SONET jitter specifications, does not require an external reference clock to aid in frequency acquisition, and provides excellent tolerance to both deterministic and sinusoidal jitter. The MAX3873A provides a PLL loss-of-lock (active-low LOL) output to indicate whether the CDR is in lock. The recovered data and clock outputs are CML with on-chip 50 back terminations on each line. The clock output can be powered down if not used. The MAX3873A is implemented in Maxim's second-generation SiGe process and consumes only 260mW at 3.3V supply (output clock disabled, low output swing). The device is available in a 4mm x 4mm 20-pin QFN exposed-pad package and operates from -40°C to +85°C.

II. Manufacturing Information

A. Description/Function:	Low-Power, Compact 2.5Gbps/2.7Gbps Clock-Recovery and Data-Retiming IC
B. Process:	G4
C. Number of Device Transistors:	
D. F abrication Location:	Oregon
E. Assembly Location:	China, Thailand
F. Date of Initial Production:	July 23, 2001

III. Packaging Information

A. Package Type:	20-pin TQFN 4x4
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-2621
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	59°C/W
K. Single Layer Theta Jc:	5.7°C/W
L. Multi Layer Theta Ja:	39°C/W
M. Multi Layer Theta Jc:	5.7°C/W

IV. Die Information

A. Dimensions:	80 X 80 mils
B. Passivation:	Si_3N_4
C. Interconnect:	Au
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn) Metal 1, 2 & 3 5.6 microns (as drawn) Metal 4
F. Minimum Metal Spacing:	1.6 microns (as drawn) Metal 1, 2 & 3, 4.2 microns (as drawn) Metal 4
G. Bondpad Dimensions:	5 mil. Sq.
H. I solation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Managing Director of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. S ampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{4.045}{192 \times 4340 \times 233 \times 2}$$

(Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 10.4 \times 10^{-9}$

λ = 10.4 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim"s reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the G4 Process results in a FIT Rate of 0.02 @ 25C and 0.37 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot N1804504B, D/C 0309)

The HF80 die type has been found to have all pins able to withstand a HBM transient pulse of +/-400V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

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Table 1
Reliability Evaluation Test Results

MAX3873AETP+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C	DC Parameters	48	0	N180F3506DQ, DC 0505
	Biased	& functionality	50 0		N180E4504BQ, DC 0437
	Time = 192 hrs.		45	0	N180D4504BQ, DC 0309
			45 0		N180C3505CQ, DC 0203
			45	0	N180B4224DQ, DC 0117

Note 1: Life Test Data may represent plastic DIP qualification lots.

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