RELIABILITY REPORT

FOR

MAX3872EGJ+

PLASTIC ENCAPSULATED DEVICES

January 5, 2010

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
Director, Reliability Engineering

Conclusion

The MAX3872EGJ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim''s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim''s quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX3872 is a compact, multirate clock and data recovery with limiting amplifier for OC-3, OC-12, OC-24, OC-48, OC-48 with FEC SONET/SDH and Gigabit Ethernet (1.25Gbps/2.5Gbps) applications. Without using an external reference clock, the fully integrated phase-locked loop (PLL) recovers a synchronous clock signal from the serial NRZ data input. The input data is then retimed by the recovered clock, providing a clean data output. An additional serial input (SLBI±) is available for system loopback diagnostic testing. Alternatively, this input can be connected to a reference clock to maintain a valid clock output in the absence of data transitions. The device also includes a loss-of-lock (active-low LOL) output. The MAX3872 contains a vertical threshold control to compensate for optical noise due to EDFAs in DWDM transmission systems. The recovered data and clock outputs are CML with on-chip 50 back termination on each line. Its jitter performance exceeds all SONET/SDH specifications. The MAX3872 operates from a single +3.3V supply and typically consumes 580mW. It is available in a 5mm x 5mm 32-pin thin QFN with exposed-pad package and operates over a -40°C to +85°C temperature range.

II. Manufacturing Information

A. Description/Function:	Multirate Clock and Data Recovery with Limiting Amplifier
B. Process:	G4
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon
E. Assembly Location:	Korea
F. Date of Initial Production:	January 15, 2003

III. Packaging Information

A. Package Type:	32-pin QFN 5x5
B. Lead Frame:	Copper
C. Lead Finish:	Matte Sn plate 100%
D. Die Attach:	Conductive
E. Bondwire:	Au (1.2 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-4101-0009
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	47°C/W
K. Single Layer Theta Jc:	2.3°C/W
L. Multi Layer Theta Ja:	30°C/W
M. Multi Layer Theta Jc:	2.3°C/W

IV. Die Information

A. Dimensions:	93 X 95 mils
B. Passivation:	Si_3N_4
C. Interconnect:	Au
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn) Metal 1, 2 & 3 5.6 microns (as drawn) Metal 4
F. Minimum Metal Spacing:	1.6 microns (as drawn) Metal 1, 2 & 3, 4.2 microns (as drawn) Metal 4
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 93 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 11.6 \times 10^{-9}$

λ = 11.6 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim"s reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the G4 Process results in a FIT Rate of 0.02 @ 25C and 0.37 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The HT19 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500 V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250 mA.

Table 1
Reliability Evaluation Test Results

MAX3872EGJ

TEST ITEM	**TEST CONDITION**	**FAILURE IDENTIFICATION**	**SAMPLE SIZE**	**NUMBER OF FAILURES**
Static Life Test (Note 1)				
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality	93	0
Moisture Testing (Note 2)				
HAST	Ta = 130°C RH = 85% Biased Time = 96hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data