RELIABILITY REPORT

FOR

MAX3825U/D

PLASTIC ENCAPSULATED DEVICES

October 4, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX3825 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX3825 is a quad transimpedance amplifier (TIA) intended for 2.5Gbps system interconnect applications. Each of the four channels converts a small photodiode current to a measurable differential voltage with a transimpedance gain of 3.7kohm. The circuit features 460nA$_{RMS}$ of input-referred noise per channel corresponding to an optical input sensitivity of -22.3dBm (BER $\leq$ 1 x 10^{-14}). The quad transimpedance amplifier has 20ps of deterministic jitter and a 2.4GHz small-signal bandwidth. The MAX3825 is optimized for use with a quad PIN photodetector array with a standard fiber pitch of 250µm.

The MAX3825 operates from a single +3.3V supply over a 0°C to +85°C temperature range. With a +3.3V supply, each channel dissipates 93mW of power. A DC cancellation circuit on each channel provides a true differential output swing over a wide range of input currents.

Each channel has an independent supply and ground to allow all or any combination of channels to be connected. This device is available in dice only.

B. Absolute Maximum Ratings

Item	Rating
Supply Voltage VCCO1, VCCO2, VCCO3, VCCO4, VCCI1, VCCI2, VCCI3, VCCI4, VCCFILT	-0.5V to +6.0V
Input Current: IN1, IN2, IN3, IN4	-4mA to +4mA
FILTER Current	-24mA to +24mA
Filter Current: FILT1, FILT2, FILT3, FILT4	-6mA to +6mA
Output Voltage OUT1±, OUT2±, OUT3±, OUT4±	(VCC - 1.5V) to (VCC + 0.5V)
ENABLE Voltage	-0.5V to (VCC + 0.5V)
Operating Temperature Range (TA)	0°C to +85°C
Storage Temperature Range	-55°C to +150°C
Operating Junction Temperature (TJ)	-55°C to +150°C
Processing Temperature	+400°C

II. Manufacturing Information

A. Description/Function:	+3.3V, 2.5Gbps Quad Transimpedance Amplifier for System Interconnects
B. Process:	GST2 (High-Speed Double Poly-Silicon Bipolar Process)
C. Number of Device Transistors:	1469
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Korea
F. Date of Initial Production:	October, 2000

III. Packaging Information

A. Package Type:	**Die Only**
B. Lead Frame:	n/a
C. Lead Finish:	n/a
D. Die Attach:	n/a
E. Bondwire:	n/a
F. Mold Material:	n/a
G. Assembly Diagram:	n/a
H. Flammability Rating:	n/a
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	n/a

IV. Die Information

A. Dimensions:	90 x 65 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Poly / Au
D. Backside Metallization:	None
E. Minimum Metal Width:	1.4 microns (as drawn)
F. Minimum Metal Spacing:	1.4 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord	(Reliability Lab Manager)
Bryan Preeshl	(Executive Director of QA)
Kenneth Huening	(Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 9823 \times 45 \times 2}$$

(Chi square value for MTTF upper limit)

↳ Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 10.78 \times 10^{-9}$ $\lambda = 10.78$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (#06-6953) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The HF64 die type has been found to have all pins able to withstand a transient pulse of ±400V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA and/or ±20V

Table 1
Reliability Evaluation Test Results

MAX3825U/D

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 150°C Biased Time = 192 hrs. Junction Temperature = 150°C	DC Parameters & functionality	45	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	n/a	n/a
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data represents plastic TQFP package for qualification
Note 2: Generic Process Data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

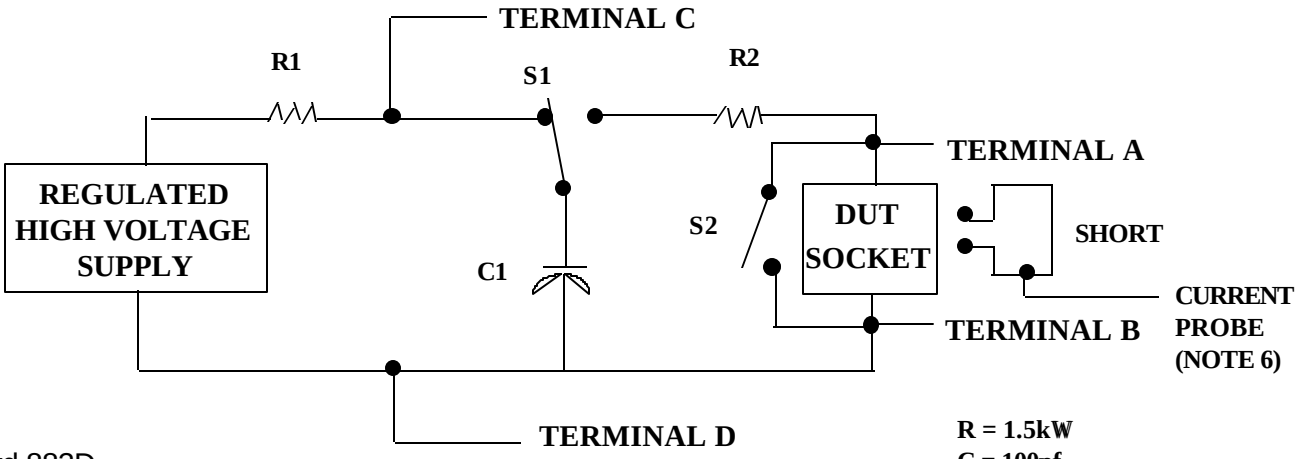
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8