RELIABILITY REPORT

FOR

MAX3761EEP

PLASTIC ENCAPSULATED DEVICES

April 30, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX3761 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX3761 limiting amplifier, with 4mV sensitivity and PECL data output, is optimized for operation in low-cost, 622Mbps, LAN/ATM LAN fiber optics applications.

An integrated power detector senses the input signal's amplitude. A received-signal-strength indicator (RSSI) gives an analog indication of the power level, while the complementary loss-of-signal (LOS) outputs indicate if the input power level exceeds the programmed threshold level. The LOS threshold can be adjusted to detect signal amplitudes between 3mVp-p and 100mVp-p, providing a 15dB LOS adjustment in fiber optic receivers. The LOS outputs have 3.5dB of hysteresis, which prevents chatter when input signal levels are small. The MAX3761's LOS outputs are compatible with TTL-logic levels.

DISABLE and LOS can be used to implement a squelch function, which turns off the data outputs when the input signal is below the programmed threshold.

B. Absolute Maximum Ratings

Item	Rating
V_{CC}, VCCO	-0.5V to +7.0V
FILTER, RSSI, EN, VIN+, VIN-, CZP, CZN, DISABLE, LOS+, LOS-, INV, VTH	-0.5V to (V_{CC} + 0.5V)
PECL Output Current (OUT+, OUT-, LOS+, LOS-)	50mA
Storage Temp.	-65°C to +160°C
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation (TA = +70°C)	
24-Pin SSOP	667mW
Derate above +70°C	
24-Pin SSOP	8.3mW/°C

II. Manufacturing Information

A. Description/Function:	Low-Power, 622Mbps Limiting Amplifier with Chatter-Free Power Detect for LANs
B. Process:	GST-2 - High Speed Double Poly-Silicon Bipolar Process
C. Number of Device Transistors:	961
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Korea, Philippines, Thailand or Malaysia
F. Date of Initial Production:	June, 1996

III. Packaging Information

A. Package Type:	**20-Lead QSOP**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-7001-0209
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

IV. Die Information

A. Dimensions:	59 x 63 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Poly / Au
D. Backside Metallization:	None
E. Minimum Metal Width:	1.4 microns (as drawn)
F. Minimum Metal Spacing:	1.4 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director**)**
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 9823 \times 40 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 12.13 \times 10^{-9}$

$\lambda = 12.13$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-B3A**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The HF10Z die type has been found to have all pins able to withstand a transient pulse of ±1000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). This product will experience permanent latch conditions when an external stimulus of ±50mA is applied to any input/output lead. However, if absolute maximum ratings are followed (reference section I), no latchup is observed.

Table 1
Reliability Evaluation Test Results

MAX3761EEP

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality		40	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	QSOP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

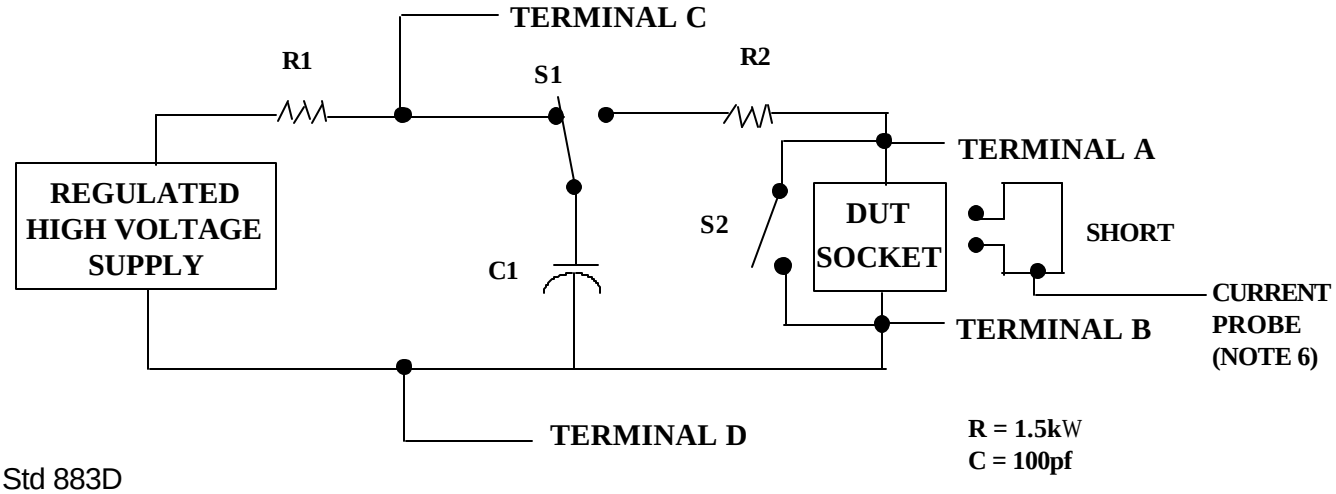
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

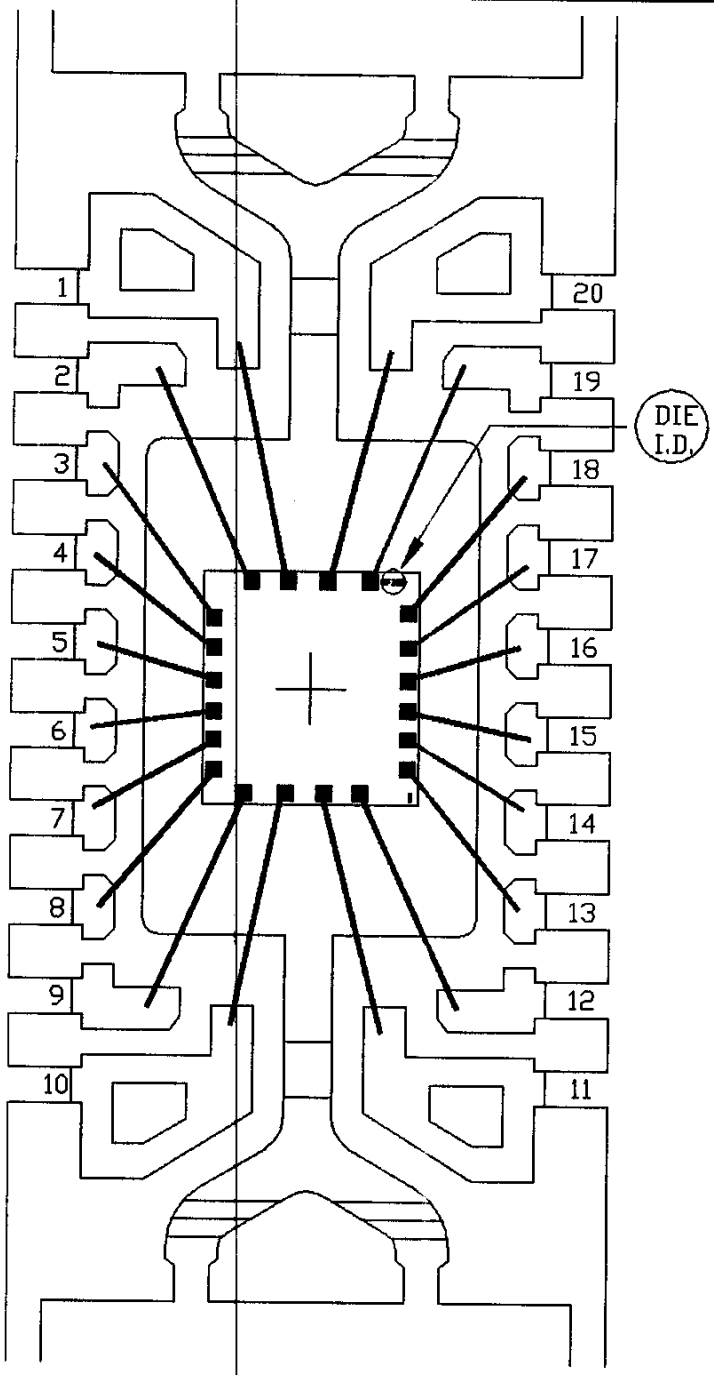
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8



PKG.CODE: E20-1		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 96X140	PKG. DESIGN			BUILDSHEET NUMBER: 05-7001-0209 / REV.: A