RELIABILITY REPORT

FOR

MAX3656ETG

PLASTIC ENCAPSULATED DEVICES

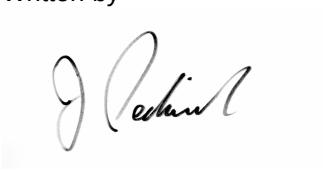
June 20, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



Jim Pedicord
Quality Assurance
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Reviewed by

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Conclusion

The MAX3656 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX3656 is a burst-mode laser driver that operates at data rates from 155Mbps up to 2.5Gbps. The laser driver accepts either positive-referenced emitter-coupled logic (PECL) or current-mode logic (CML) data inputs and provides bias and modulation current for the laser diode. The device can switch the laser diode from a completely dark (off) condition to a full (on) condition (with proper bias and modulation currents) in less than 2ns. The MAX3656 incorporates DC-coupling between laser driver and laser diode and operates with a single-supply voltage as low as +3.0V.

A digital automatic power-control (APC) loop is provided to maintain the average optical power over the full temperature range and lifetime. The APC loop is functional for a minimum burst on-time of 576ns and minimum burst off-time of 96ns, with no limit on the maximum burst on- or off-time. A fail monitor is provided to indicate when the APC loop can no longer maintain the average power. The MAX3656 can be configured for nonburst-mode applications (continuous mode) by connecting burst enable (BEN) high. For power saving, the MAX3656 provides enabling and disabling functionality. The modulation current can be set from 10mA to 85mA and the bias current can be set from 1mA to 70mA.

The MAX3656 is packaged in a small, 24-pin, 4mm x 4mm thin QFN package and consumes only 132mW (typ), excluding bias and modulation currents.

B. Absolute Maximum Ratings

Item	Rating
Supply Voltage, VCC	-0.5V to +6.0V
Current into BIAS+, BIAS-, OUT+, OUT-	-20mA to +150mA
Current into MD	-5mA to +5mA
Current into FAIL	-10mA to +10mA
Voltage at IN+, IN-, BEN+, BEN-, EN, LONGB	-0.5V to (VCC + 0.5V)
Voltage at MODSET, APCSET, BIASMAX	-0.5V to +3.0V
Voltage at OUT+, OUT-	+0.5V to (VCC + 1.5V)
Voltage at BIAS+, BIAS-	+0.5V to (VCC + 0.5V)
Operating Ambient Temperature Range (TA)	-40°C to +85°C
Operating Junction Temperature Range (TJ)	-55°C to +150°C
Storage Ambient Temperature Range (TSTG)	-55°C to +150°C
Processing Temperature (die)	+400°C
Lead Temperature (soldering,10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
24-Pin Thin QFN-EP	1805mW
Derates above +70°C	
24-Pin Thin QFN-EP	27.8mW/°C

II. Manufacturing Information

A. Description/Function:	155Mbps to 2.5Gbps Burst-Mode Laser Driver
B. Process:	GST4-F60
C. Number of Device Transistors:	8153
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Thailand
F. Date of Initial Production:	March, 2003

III. Packaging Information

A. Package Type:	**24-Pin QFN-EP (4x4)**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled epoxy
E. Bondwire:	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-9000-0473
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

IV. Die Information

A. Dimensions:	98 x 65 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Au
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1: 1.2; Metal2: 1.2; Metal3: 1.2; Metal4: 5.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1: 1.6; Metal2: 1.6; Metal3: 1.6; Metal4: 4.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 9823 \times 44 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 11.03 \times 10^{-8}$ $\lambda = 11.03$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The Burn-In Schematic (Spec.# 06-7123) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Reports (**RR-1M** & **RR-B3A**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The HD43 die type has been found to have all pins able to withstand a transient pulse of +/-1000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX3656ETG

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality	44	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic process/package data.

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

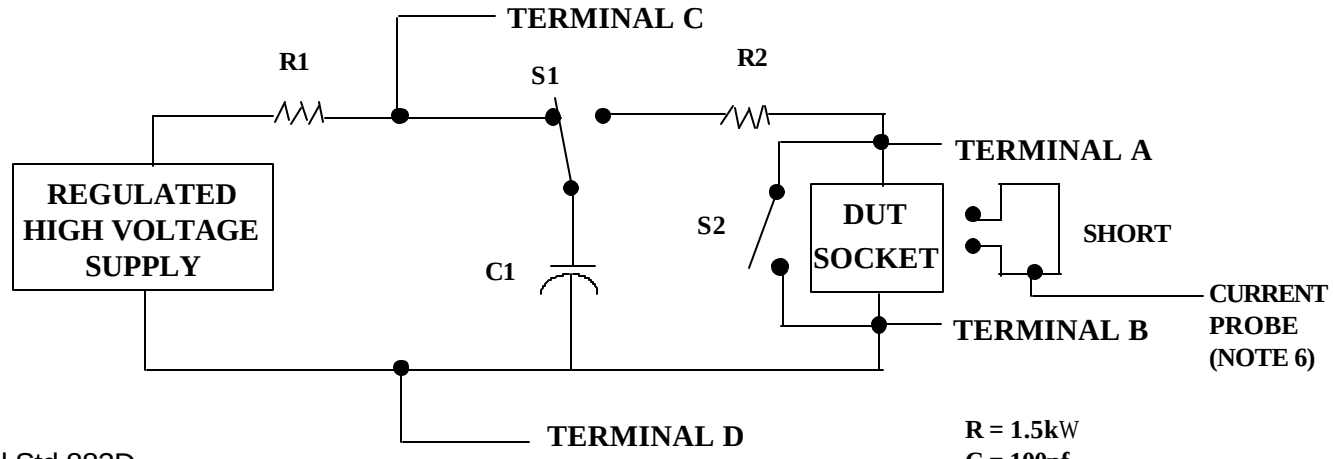
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

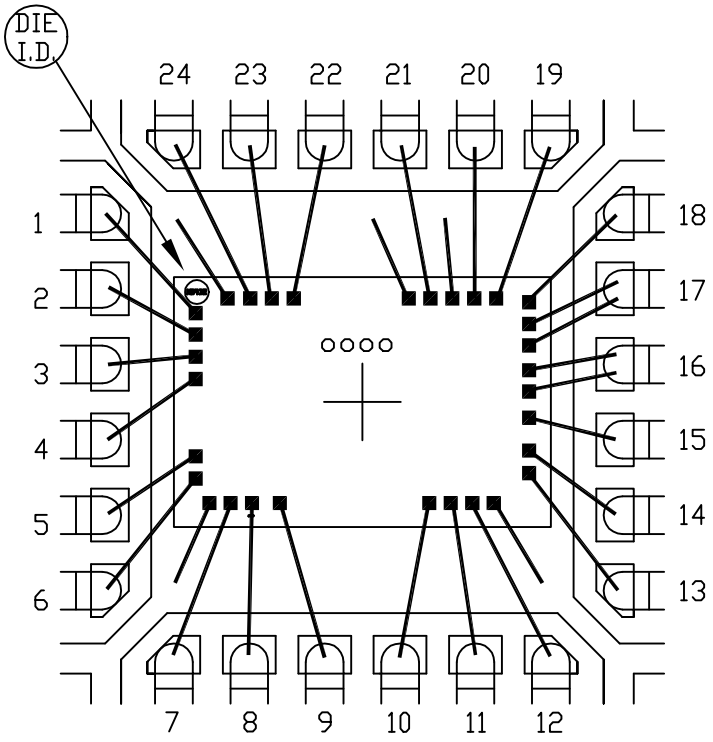
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8

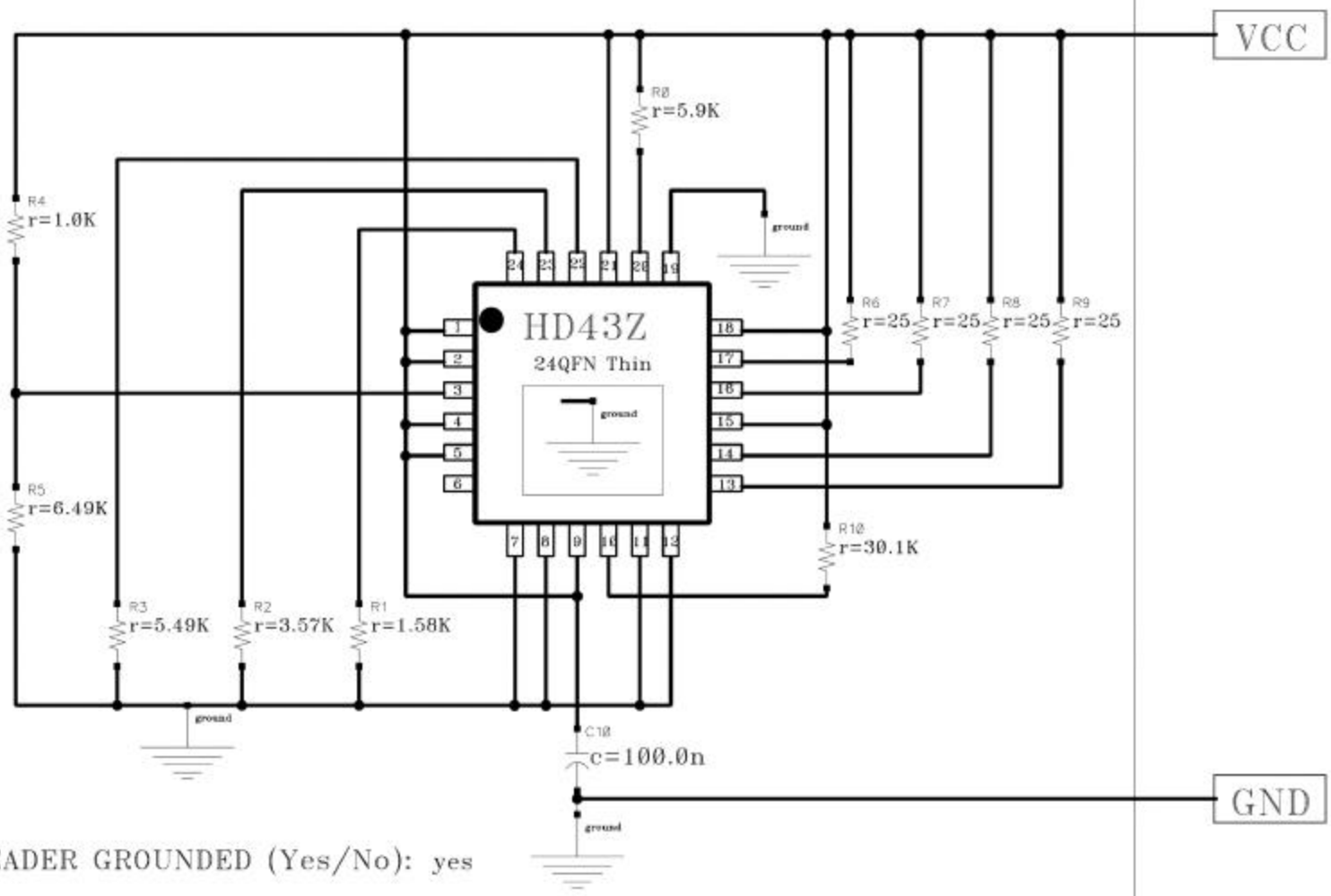
4x4x0.8 MM QFN THIN PKG. EXPOSED PAD PKG.



PKG. CODE: T2444-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 110×110	PKG.			BOND DIAGRAM #: 05-9000-0473	REV: A
	DESIGN				

ONCE PER SOCKET

ONCE PER BOARD



HEADER GROUNDED (Yes/No): yes

PRODUCT: MAX 3656 PACKAGE TYPE: 24QFN Thin-EP 4.0x4.0x0.8 mm	DRAWN BY:
VERSION #: DATE : Oct 4 10:08:33 2002	NOTES: Exposed paddle must be connected to ground. HD43Z daughter card
ICC (MAX) : 220mA	
VCC : 3.6 VOLTS	

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