

RELIABILITY REPORT FOR MAX3643ETG+T PLASTIC ENCAPSULATED DEVICES

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MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR. SUNNYVALE, CA 94086

Approved by	
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Conclusion

The MAX3643ETG+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

- I.Device Description V.Quality Assurance Information
- II.Manufacturing Information
- III.Packaging Information

- VI.Reliability Evaluation
-Attachments

IV.Die Information

I. Device Description

A. General

The MAX3643 burst-mode laser driver provides bias and modulation current drive for PON burst-mode ONT applications. It is specifically designed for use with a low-cost external controller for the APC (and if desired, AMC) loop. A high-speed differential burst-enable input enables the driver to switch the laser from a dark (output off) condition to full on condition in less than 2ns. When BEN is inactive, typical modulation and bias currents are 5µA each. Laser modulation current can be set from 10mA to 85mA and bias current can be set from 1mA to 70mA using the MODSET and BIASSET inputs. A sample-and-hold circuit is provided to capture the monitor diode output during short PON bursts, if needed, and the BEN high-speed signal is mirrored on an LVCMOS output to be used by the controller operating the APC/AMC loop. The MAX3643 burst-mode laser driver is packaged in a 4mm x 4mm, 24-pin thin QFN package. It operates from -40°C to +85°C.



II. Manufacturing Information

A. Description/Function: 155Mbps to 2.5Gbps Burst-Mode Laser Driver
B. Process: CB53
C. Number of Device Transistors: 3123
D. Fabrication Location: USA
E. Assembly Location: China, Taiwan and Thailand
F. Date of Initial Production: October 22, 2005

III. Packaging Information

A. Package Type:	24-pin TQFN 4x4
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4487
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	48°C/W
K. Single Layer Theta Jc:	3°C/W
L. Multi Layer Theta Ja:	36°C/W
M. Multi Layer Theta Jc:	3°C/W

IV. Die Information

Α.	Dimensions:	88.98 x 57.87 mils
В.	Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C.	Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D.	Backside Metallization:	None
E.	Minimum Metal Width:	Metal1 = 0.6 / Metal2 = 0.6 / Metal3 = 1.2 microns (as drawn)
F.	Minimum Metal Spacing:	Metal1 = 0.4 / Metal2 = 0.4 / Metal3 = 1.2 microns (as drawn)
G.	Bondpad Dimensions:	
Н.	Isolation Dielectric:	SiO ₂
I.	Die Separation Method:	Wafer Saw



V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 123C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

 $\lambda = \underbrace{1}_{\text{MTTF}} = \underbrace{\frac{1.83}_{192 \times 4340 \times 80 \times 2}}_{(\text{where } 4340 = \text{Temperature Acceleration factor assuming an activation energy of 0.8eV})$ $\lambda = 27.3 \times 10^{-9}$ $\lambda = 27.3 \text{ F.I.T. (60\% confidence level @ 25°C)}$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the CB53 Process results in a FIT Rate of 0.46 @ 25C and 7.85 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot J0UZB4001B, D/C 1113)

The HQ43 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.



Table 1 Reliability Evaluation Test Results

MAX3643ETG+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS			
Static Life Test (Note 1)								
	Ta = 123C	DC Parameters	48	0	J0UZB4001B, D/C 1131			
	Biased	& functionality	32	0	J0UZB4001C, D/C 1131			
	Time = 192 hrs.							

Note 1: Life Test Data may represent plastic DIP qualification lots.