RELIABILITY REPORT

FOR

MAX3380ECUP
PLASTIC ENCAPSULATED DEVICES

May 17, 2007

MAXIM INTEGRATED PRODUCTS

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Approved by
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Conclusion

The MAX3380E successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX3380E/MAX3381E are +2.35V to +5.5V-powered EIA/TIA-232 and V.28/V.24 communication interfaces with low power requirements, high data-rate capabilities, and enhanced electrostatic discharge (ESD) protection on both the TTL and RS-232 sides. The MAX3380E/MAX3381E have two receivers and two transmitters. All RS-232 inputs, outputs, and logic input pins are protected to ±15kV using IEC 1000-4-2 Air-Gap Discharge method and the Human Body Model, and ±8kV using IEC 1000-4-2 Contact Discharge method.

The proprietary low-dropout transmitter output stage enables true RS-232 performance from a +3.1V to +5.5V supply with a dual charge pump. The parts reduce the transmitter output levels to RS-232-compatible levels with no increase in supply current for supplies less than +3.1V and greater than +2.35V. The +2.35V to +5.5V operating range is fully compatible with lithium-ion (Li+) batteries. The charge pump requires only four small 0.1µF capacitors for operation.

The MAX3380E/MAX3381E transceivers use Maxim's revolutionary AutoShutdown Plus™ feature to automatically enter a 1µA shutdown mode. These devices shut down the on-board power supply and drivers when they do not sense a valid signal transition for 30 seconds on either the receiver or transmitter inputs.

The MAX3380E is capable of transmitting data at rates of 460kbps while maintaining RS-232 output levels, and the MAX3381E operates at data rates up to 250kbps. The MAX3381E offers a slower slew rate for applications where noise and EMI are issues. The MAX3380E/MAX3381E have a unique V_L pin that allows interoperation in mixed-logic voltage systems down to +1.65V. Both input and output logic levels are referenced to the V_L pin. The MAX3380E/MAX3381E are available in a space-saving TSSOP package.

B. Absolute Maximum Ratings

Item	Rating
VCC to GND	-0.3V to +7V
SHDN to GND	-0.3V to (VL + 0.3V)
I/O VL to GND	-0.3V to (VL + 0.3V)
VL, I/O VCC to GND	-0.3V to (VCC + 0.3V)
Short-Circuit Duration: I/O VL, I/O VCC to GND	Continuous
Continuous Power Dissipation (TA = +70°C)	
SC70 (derate 3.1mW/°C above +70°C)	245mW
6-Pin µDFN (derate 2.1mW/°C above +70°C)	168mW
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

II. Manufacturing Information

A. Description/Function:	**+2.35V to +5.5V, 1µA, 2Tx/2Rx RS-232 Transceivers with ±15kV ESD - Protected I/O and Logic Pins**
B. Process:	S3
C. Number of Device Transistors:	1476
D. Fabrication Location:	California, USA
E. Assembly Location:	Philippines
F. Date of Initial Production:	July 2001

III. Packaging Information

A. Package Type:	**20-Lead TSSOP**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate or 100% Matte Tin
D. Die Attach:	Silver-Filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-2601-0045
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1

IV. Die Information

A. Dimensions:	98 x 179 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	3 microns (as drawn)
F. Minimum Metal Spacing:	3 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Ken Wendel (Director, Reliability Engineering)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are pending. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 160 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 6.87 \times 10^{-9}$

λ = 6.87 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5728) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1N**). Current monitor data for the S3 Process results in a FIT Rate of 0.12 @ 25C and 2.13 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The RT24 die type has been found to have all pins able to withstand a transient pulse of ±2500V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX3380ECUP

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		160	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality		77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

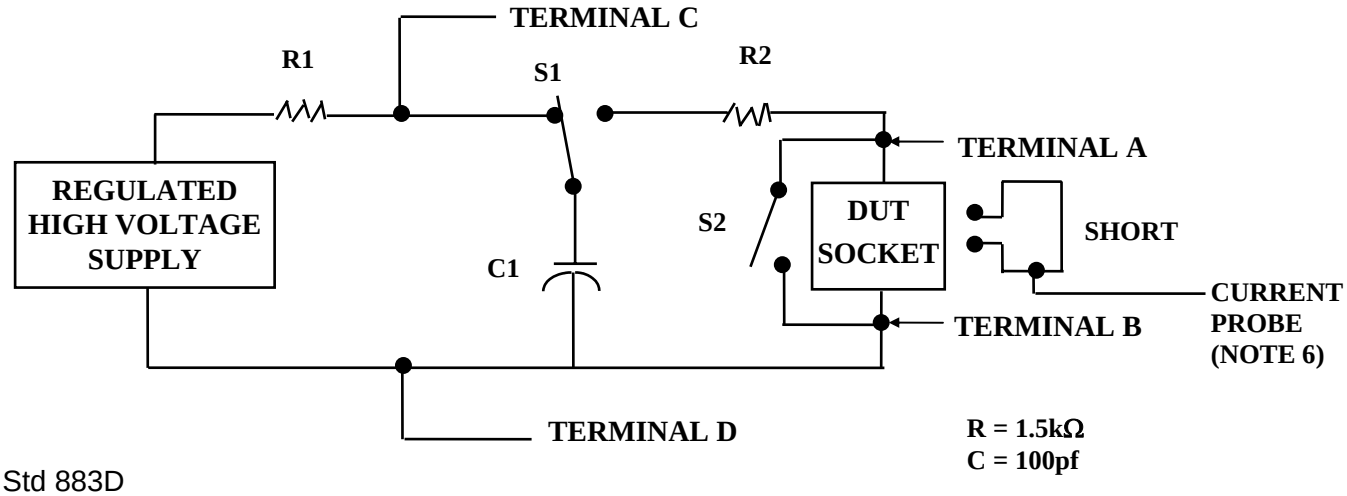
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8