RELIABILITY REPORT

FOR

MAX3273EGG

PLASTIC ENCAPSULATED DEVICES

January 14, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX3273 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX3273 is a compact, low-power laser driver for applications up to 2.7Gbps. The device uses a single +3.3V supply and typically consumes 30mA. The bias and modulation current levels are programmed by external resistors. An automatic power-control (APC) loop is incorporated to maintain a constant average optical power over temperature and lifetime. The laser driver is fabricated using Maxim's in-house second generation SiGe process.

The MAX3273 accepts differential CML-compatible clock and data input signals. Inputs are self-biased to allow AC-coupling. An input data-retiming latch can be enabled to reject input jitter if a clock signal is available.

The driver can provide bias current up to 100mA and modulation current up to 60mAp-p with typical (20% to 80%) edge speeds of 59ps. A failure-monitor output is provided to indicate when the APC loop is unable to maintain average optical power. The MAX3273 is available in a 4mm 5 4mm, 24-pin QFN package, as well as in die form

B. Absolute Maximum Ratings

<u>ltem</u>	Rating
Supply Voltage, VCC	-0.5V to +6.0V
Current into BIAS, OUT+, OUT-	-20mA to +150mA
Current into MD	-5mA to +5mA
Voltage at DATA+, DATA-, CLK+,CLK-, LATCH, EN , FAIL	-0.5V to (VCC + 0.5V)
Voltage at MODSET, BIASMAX, APCSET, APCFILT1, APCFILT2	` ,
Voltage at BIAS	+1.0V to (VCC + 1.5V)
Voltage at OUT+, OUT-	+1.5V to (VCC + 1.5V)
Current into FAIL	-10mA to +10mA
Continuous Power Dissipation (TA = +85°C)	101111110
24-Pin QFN	1781mW
Derates above +85°C	
24-Pin QFN	27.4mW/°C
Storage Temperature Range	-55°C to +150°C
Operating Junction Temperature	-55°C to +150°C
Die Attach Temperature (die)	+400°C
Lead Temperature (soldering, 10s)	+300°C

II. Manufacturing Information

A. Description/Function: +3.3V, 2.5Gbps Low-Power Laser Driver

B. Process: GST4-F60

C. Number of Device Transistors: 1672

D. Fabrication Location: Oregon, USA

E. Assembly Location: Korea

F. Date of Initial Production: July, 2001

III. Packaging Information

A. Package Type: 24-Pin QFN (4x4)

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: Silver-filled epoxy

E. Bondwire: Gold (1.2 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: Buildsheet # 05-7001-0534

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per

JEDEC standard JESD22-A112: Level 1

IV. Die Information

A. Dimensions: 79 x 64 mils

B. Passivation: Si₃N₄/SiO₂ (Silicon nitride/ Silicon dioxide)

C. Interconnect: Au

D. Backside Metallization: None

E. Minimum Metal Width: Metal1: 1.2; Metal2: 1.2; Metal3: 1.2; Metal4: 5.6 microns (as drawn)

F. Minimum Metal Spacing: Metal1: 1.6; Metal2: 1.6; Metal3: 1.6; Metal4: 4.2 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO₂

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)

Bryan Preeshl (Executive Director of QA)

Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 9823 \times 45 \times 2}$$
 (Chi square value for MTTF upper limit)
$$\lambda = \frac{1}{192 \times 9823 \times 45 \times 2}$$
Temperature Acceleration factor assuming an activation energy of 0.8eV
$$\lambda = 10.78 \times 10^{-8}$$

$$\lambda = 10.78 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Reports (RR-1M & RR-B3A).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The HD11 die type has been found to have all pins able to withstand a transient pulse of \pm 00V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of \pm 250mA.

Table 1Reliability Evaluation Test Results

MAX3273EGG

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Tes	t (Note 1)			
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality	45	0
Moisture Testi	ng (Note 2)			
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical St	ress (Note 2)			
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic process/package data.

Attachment #1

TABLE II. Pin combination to be tested. 1/2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V _{PS1} 3/	All V _{PS1} pins
2.	All input and output pins	All other input-output pins

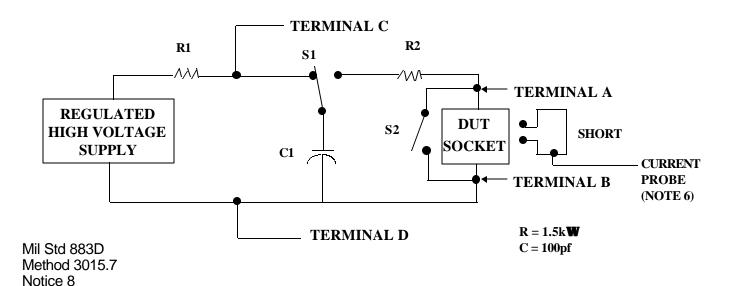
- Table II is restated in narrative form in 3.4 below.
- No connects are not to be tested.

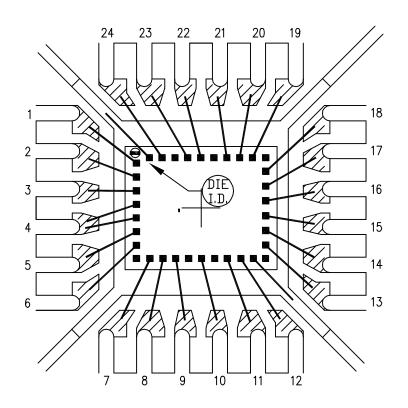
 Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_{S_1}$, $-V_{S_1}$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- Each pin individually connected to terminal A with respect to the device ground pin(s) connected to a. terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- Each pin individually connected to terminal A with respect to each different set of a combination of b. all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- Each input and each output individually connected to terminal A with respect to a combination of all c. the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





BONDABLE AREA

PKG. BODY SIZE: 4×4 mm

PKG. CODE: G2444-1		SIGNATURES	DATE	CONFIDENTIAL & PROPRIE	
CAV./PAD SIZE:	PKG.			BOND DIAGRAM #:	REV:
91×91	DESIGN			05-7001-0534	Α

