RELIABILITY REPORT

FOR

**MAX3268CUB**

PLASTIC ENCAPSULATED DEVICES

January 26, 2001

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

Jim Pedicord
Quality Assurance
Reliability Lab Manager

Reviewed by

Bryan J. Preeshl
Quality Assurance
Executive Director

## Conclusion

The MAX3268 Successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

## Table of Contents



## I. Device Description

### A. General

The 1.25Gbps MAX3268 limiting amplifiers is designed for Gigabit Ethernet and Fibre Channel optical receiver systems. The amplifier accepts a wide range of input voltages and provide constant-level output voltages with controlled edge speeds. Additional features include RMS power detectors with programmable loss-of-signal (LOS) indication, an optional squelch function that mutes the data output signal when the input voltage falls below a programmable threshold, and excellent jitter performance.

The MAX3268 features standards-compliant positive-referenced emitter-coupled logic (PECL) data outputs and is available in a tiny 10-pin µMAX package that is ideal for small-form-factor receivers.

### B. Absolute Maximum Ratings

| Item | Rating |
|---|---|
| Supply Voltage (VCC ) | -0.5V to +6V |
| Voltage at IN+, IN- | (VCC – 2.4V) to (VCC + 0.5V) |
| Voltage at SQELCH, CAZ1, CAX2, LOS, /LOS, TH | -0.5V to (VCC + 0.5V) |
| Voltage at LEVEL | -0.5V to +2.0V |
| Current in LOS, /LOS | -1mA to +9mA |
| Differential Input Voltage (IN+ - IN-) | 2.5V |
| Continuous Current at CML Outputs (OUT+, OUT-) | -25mA to +25mA |
| Continuous Current at PECL Outputs (OUT+, OUT-) | 50mA |
| Storage Temperature Range | -55°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Continuous Power Dissipation | |
| 10-Pin µMAX | 1600mW |
| Derates above +70°C | |
| 10-Pin µMAX | 20mW/°C |

## II. Manufacturing Information

A. Description/Function: 3.0V to 5.5V, 1.25Gbps Limiting Amplifiers

B. Process: GST2 – High Speed Double Poly-Silicon Bipolar Process

C. Number of Device Transistors: 728

D. Fabrication Location: Oregon, USA

E. Assembly Location: Malaysia

F. Date of Initial Production: January, 2000

## III. Packaging Information

A. Package Type: **10-Lead uMax**

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: Silver-filled Epoxy

E. Bondwire: Gold (1.0 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: Buildsheet # 05-7001-0390

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1

## IV. Die Information

A. Dimensions: 61 x 61

B. Passivation: $Si_3N_4/SiO_2$ (Silicon nitride/ Silicon dioxide)

C. Interconnect: Poly / Au

D. Backside Metallization: None

E. Minimum Metal Width: 2 microns (as drawn)

F. Minimum Metal Spacing: 2 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: $SiO_2$

I. Die Separation Method: Wafer Saw

## V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ($\lambda$) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 9823 \times 45 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 10.78 \times 10^{-9}$ $\lambda = 10.78$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**) located on the Maxim website at http://www.maxim-ic.com .

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The HF59-1 die type has been found to have all pins able to withstand a transient pulse of ±1500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA and/or ±20V.

**Table 1**
Reliability Evaluation Test Results

## MAX3268CUB

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | SAMPLE SIZE | NUMBER OF FAILURES |
|---|---|---|---|---|
| **Static Life Test** (Note 1) | | | | |
| | Ta = 150°C<br>Biased<br>Time = 192 hrs. | DC Parameters<br>& functionality | 45 | 0 |
| **Moisture Testing** (Note 2) | | | | |
| Pressure Pot | Ta = 121°C<br>P = 15 psi.<br>RH= 100%<br>Time = 168hrs. | DC Parameters<br>& functionality | 77 | 0 |
| 85/85 | Ta = 85°C<br>RH = 85%<br>Biased<br>Time = 1000hrs. | DC Parameters<br>& functionality | 77 | 0 |
| **Mechanical Stress** (Note 2) | | | | |
| Temperature Cycle | -65°C/150°C<br>1000 Cycles<br>Method 1010 | DC Parameters | 77 | 0 |

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic Process/Package Data

TABLE II. Pin combination to be tested. 1/ 2/

| | Terminal A (Each pin individually connected to terminal A with the other floating) | Terminal B (The common combination of all like-named pins connected to terminal B) |
|---|---|---|
| 1. | All pins except $V_{PS1}$ 3/ | All $V_{PS1}$ pins |
| 2. | All input and output pins | All other input-output pins |

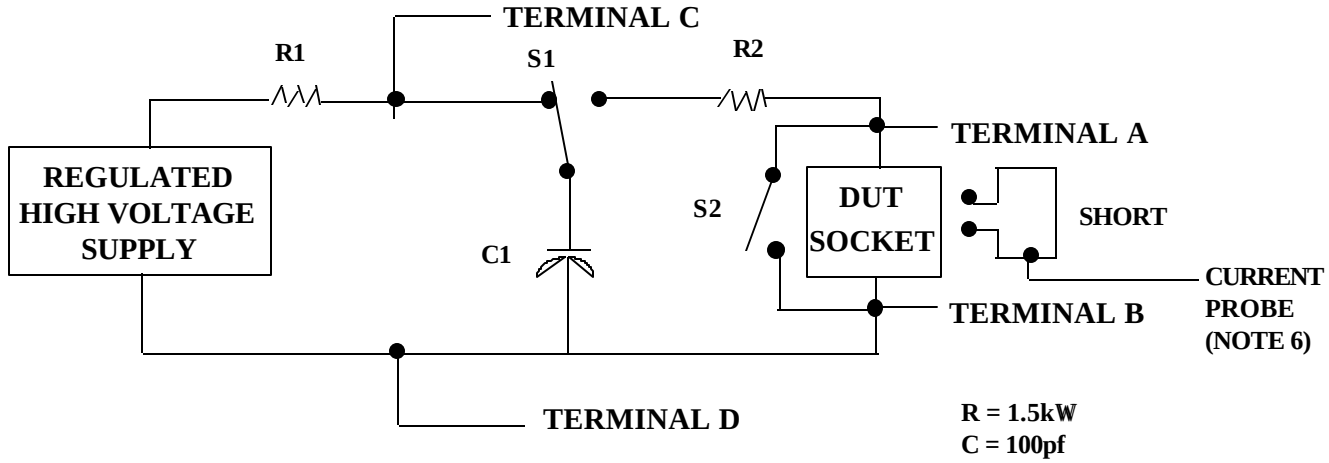
1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where $V_{PS1}$ is $V_{DD}$, $V_{CC}$, $V_{SS}$, $V_{BB}$, GND, $+V_S$, $-V_S$, $V_{REF}$, etc).

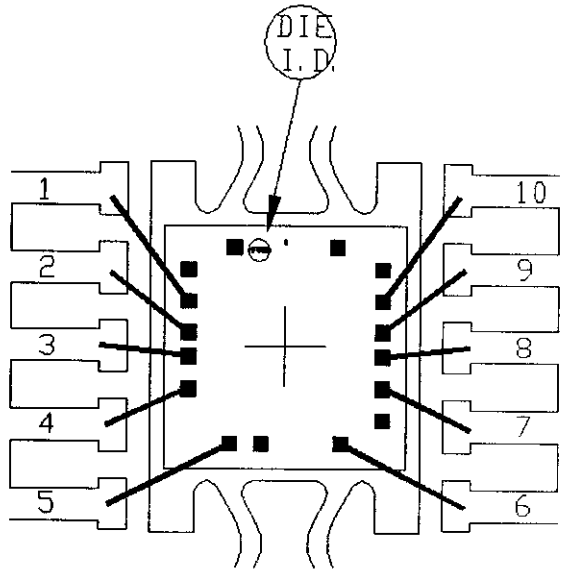
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., $V_{SS1}$, or $V_{SS2}$ or $V_{SS3}$ or $V_{CC1}$, or $V_{CC2}$) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



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|---|---|---|---|---|
| PKG. CODE: U10E-3 | | APPROVALS | DATE | MAXIM |
| CAV./PAD SIZE: 68×73 | PKG. DESIGN | | | BUILDSHEET NUMBER: 05-7001-0390 / REV.: B |