

RELIABILITY REPORT FOR MAX32552 PLASTIC ENCAPSULATED DEVICES

March 4, 2017

# **MAXIM INTEGRATED**

160 RIO ROBLES SAN JOSE, CA 95134

Eric Wright **Reliability Engineer** 

Brian Standley Manager, Reliability



#### Conclusion

The MAX32552 successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

#### **Table of Contents**

- I. ......Device Description
  II. ......Manufacturing Information

IV. .....Die Information V. .....Quality Assurance Information

- III. ......Packaging Information
- .....Attachments
- VI. ......Reliability Evaluation

### I. Device Description

A. General

DeepCover® embedded security solutions cloak sensitive data under multiple layers of advanced physical security to provide the most secure key storage possible. The DeepCover Secure microcontroller (MAX32552) provides an interoperable, secure, and cost-effective solution to build new generations of trusted devices such as mobile chip and pin pads. The MAX32552 is based on a Cortex®- M3 processor with 1MB of embedded flash, 384KB of system RAM, 8KB of battery-backed AES selfencrypted NVSRAM. In addition to a high-performance QSPI® interface for secure code execution and data storage, it includes all the essential functions of mobile POS terminal including a cryptographic engine, a true random number generator, battery-backed RTC, environmental and tamper detection circuitry, a magnetic stripe reader, a smart card controller with embedded transceiver to directly support 1.8V, 3.3V, and 5V cards, and an integrated secure keypad controller. It also provides a seamless interface to monochrome graphic displays and includes a vast array of peripherals, SPIs, UARTs, DMA, ADC, and DAC that add flexibility to control and differentiate the system design.

# II. Manufacturing Information



A. Description/Function:	DeepCover Secure ARM Cortex-M3 Flash Microcontroller
B. Process:	TS90
C. Fabrication Location:	Taiwan
D. Assembly Location:	Taiwan
E. Date of Initial Production:	December 2, 2016

# III. Packaging Information

A. Package Type:	121-ball CTBGA-Cu
B. Lead Frame:	PCB
C. Lead Finish:	SnAgCu
D. Die Attach:	Non-conductive
E. Bondwire:	CuPd (0.8 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-100497
H. Flammability Rating:	Class UL94-V0
<ol> <li>Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C</li> </ol>	Level 3
J. Single Layer Theta Ja:	N/A°C/W
K. Single Layer Theta Jc:	N/A°C/W
L. Multi Layer Theta Ja:	32.5°C/W
M. Multi Layer Theta Jc:	8.8°C/W

## IV. Die Information

A. Dimensions:	79.9212X23.622 mils
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub>
C. Interconnect:	Cu
D. Minimum Metal Width:	0.12 microns (as drawn)
E. Minimum Metal Spacing:	0.12 microns (as drawn)
F. Isolation Dielectric:	SiO <sub>2</sub>
G. Die Separation Method:	Wafer Saw



#### V. Quality Assurance Information

A. Quality Assurance Contacts:	Eric Wright (Reliability Engineering) Brian Standley (Manager, Reliability) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

#### VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (  $\lambda$ ) is calculated as follows:

 $\frac{x}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$  (Chi square value for MTTF upper limit) (where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

**𝔅** = 13.7 x 10<sup>−9</sup>

3 = 13.7 F.I.T. (60% confidence level @ 25°C)

#### B. E.S.D. and Latch-Up Testing

The ES06-0 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.



# Table 1 Reliability Evaluation Test Results

# MAX32552

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	
Static Life Test (N	Note 1)				
	Ta = 135C	DC Parameters	80	0	
	Biased	& functionality			
	Time = 192 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots.