RELIABILITY REPORT

FOR

MAX32520-BNJ+, MAX32520-BNS+,
MAX32520-BNS+T

March 24, 2020

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

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Conclusion

The MAX32520 successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX32520 incorporates Maxim's patented ChipDNA™ PUF technology. ChipDNA technology involves a physically unclonable function (PUF) that enables cost-effective protection against invasive physical attacks. Using the random variation of semiconductor device characteristics that naturally occur during wafer fabrication, the ChipDNA circuit generates a unique output value that is repeatable over time, temperature, and operating voltage. Attempts to probe or observe ChipDNA operation modifies the underlying circuit characteristics, preventing discovery of the unique value used by the chip cryptographic functions.

The MAX32520 utilizes the ChipDNA output as key content to cryptographically secure all device stored data including user firmware. User firmware encryption provides ultimate software IP protection. The ChipDNA canalso generate a private key for the ECDSA signing operation.

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II. Manufacturing Information

A. Description/Function:	ChipDNA Secure Arm Cortex M4 Microcontroller
B. Process:	TS40
C. Device Count:	56204543
D. Fabrication Location:	Taiwan
E. Assembly Location:	Taiwan
F. Date of Initial Production:	September 20, 2019

III. Packaging Information

A. Package Type:	TQFN-CU
B. Lead Frame:	CU194
C. Lead Finish:	Matte Tin
D. Die Attach:	EN4900G
E. Bondwire:	CuPd 0.80 mil
F. Mold Material:	G700LA
G. Assembly Diagram:	05-101251
H. Flammability Rating:	UL-94 (V-0 Rating)
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	47 °C7/W
K. Single Layer Theta Jc:	1.7 °C/W
L. Multi Layer Theta Ja:	29 °C/W
M. Multi Layer Theta Jc:	1.7 °C/W

IV. Die Information

A. Dimensions:	103.559 x 104.032 mils
B. Passivation:	SiO/SiN

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V. Quality Assurance Information

A. Quality Assurance Contacts: Veronica Mercado (Engineer, Reliability)
Ryan Wall (Manager, Reliability)
Bryan Preeshl (SVP of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 125C biased (static) life test are shown in Table 1. Using these results, the Failure Rate λ is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192\ x\ 2454\ x\ 77\ x\ 2}$$ (Chi square value for MTTF upper limit)

(where 2454 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 25.2\ x\ 10^{-9}$
$\lambda = 25.2\ FITs\ (60\%\ confidence\ level\ @25°C)$

Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at https://www.maximintegrated.com/en/support/qa-reliability/reliability/reliability-monitor-program.html.

TS40 cumulative process data:
$\lambda = 1.5\ FITs\ (60\%\ confidence\ level\ @25°C)$
$\lambda = 18.0\ FITs\ (60\%\ confidence\ level\ @55°C)$

B. E.S.D. and Latch-Up Testing

The MAX32520 has been found to have all pins able to withstand an HBM transient pulse of +/- 2500 V per JEDEC / ESDA JS-001. Latch-Up testing has shown that this device withstands +/- 250 mA current injection and supply overvoltage per JEDEC JESD78.

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Table 1
Reliability Evaluation Test Results

MAX32520-BNS+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 125C Biased Time = 192 hrs.	DC Parameters & functionality	77	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.

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