

RELIABILITY REPORT
FOR
MAX3243xxl
PLASTIC ENCAPSULATED DEVICES

July 5, 2005

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX3243 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX3243* achieve 1 μ A supply current with Maxim's revolutionary AutoShutdown™ feature. When the MAX3243 do not sense a valid signal level on their receiver inputs, the on-board power supply and drivers shut down. This occurs if the RS-232 cable is disconnected or if the transmitters of the connected peripheral are turned off. The system turns on again when a valid level is applied to any RS-232 receiver input. As a result, the system saves power without changes to the existing BIOS or operating system.

The MAX3243 transceiver is a 3V-powered EIA/TIA-232 and V.28/V.24 communications interface intended for notebook computer applications. A proprietary, high-efficiency, dual charge-pump power supply and a low-dropout transmitter combine to deliver true RS-232 performance from a single +3.0V to +5.5V supply. A guaranteed data rate of 120kbps provides compatibility with popular software for communicating with personal computers.

The MAX3243 require only 0.1 μ F capacitors in 3.3V operation, and can operate from input voltages ranging from +3.0V to +5.5V. It is ideal for 3.3V-only systems, mixed 3.3V and 5.0V systems, or 5.0V-only systems that require true RS-232 performance.

The MAX3243 3-driver/5-receiver, complete serial port is ideal for notebook or subnotebook computers. The MAX3243 includes one complementary always -active receiver. This receiver can monitor an external device (such as a modem) in shutdown, without forward biasing the protection diodes in a UART that may have V_{CC} completely removed.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
VCC	-0.3V to +6V
V+ (Note 1)	-0.3V to +7V
V- (Note 1)	+0.3V to -7V
V+ + V- (Note 1)	+13V
Input Voltages	
T_IN, FORCEOFF, FORCEON	-0.3V to +6V
R_IN	±25V
Output Voltages	
T_OUT	±13.2V
R_OUT, INVALID	-0.3V to (VCC + 0.3V)
Short-Circuit Duration	
T_OUT	Continuous
Operating Temperature Ranges	
MAX3243C_ _	0°C to +70°C
MAX3243E_ _	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (+70°C)	
28-Pin Wide SO	1000mW
28-Pin SSOP	762mW
28-Pin TSSOP	696mW
Derates above +70°C	
28-Pin Wide SO	12.5mW/°C
28-Pin SSOP	9.52mW/°C
28-Pin TSSOP	8.7mW/°C

Note 1: V+ and V- can have maximum magnitudes of 7V, but their absolute difference cannot exceed 13V.

II. Manufacturing Information

A. Description/Function:	1μA Supply-Current, True +3V to +5.5V RS-232 Transceiver with AutoShutdown
B. Process:	S3 (Standard 3 micron silicon gate CMOS)
C. Number of Device Transistors:	476
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines or Malaysia
F. Date of Initial Production:	March, 1995

III. Packaging Information

A. Package Type:	28-Lead WSO	28-Lead SSOP	28-Lead TSSOP
B. Lead Frame:	Copper	Copper	Copper
C. Lead Finish:	Solder Plate or 100% Matte Tin (all packages)		
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-1901-0052	#05-1901-0053	#05-1901-0206
H. Flammability Rating:	Class UL94-V0	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1	Level 1	Level 1

IV. Die Information

A. Dimensions:	91 x 151 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	3 microns (as drawn)
F. Minimum Metal Spacing:	3 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 960 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 1.13 \times 10^{-9} \quad \lambda = 1.13 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5167) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1N**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The RS16-1 die type has been found to have all pins able to withstand a transient pulse of $\pm 2500\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX3243xxI

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		960	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality		77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic package/process data.

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

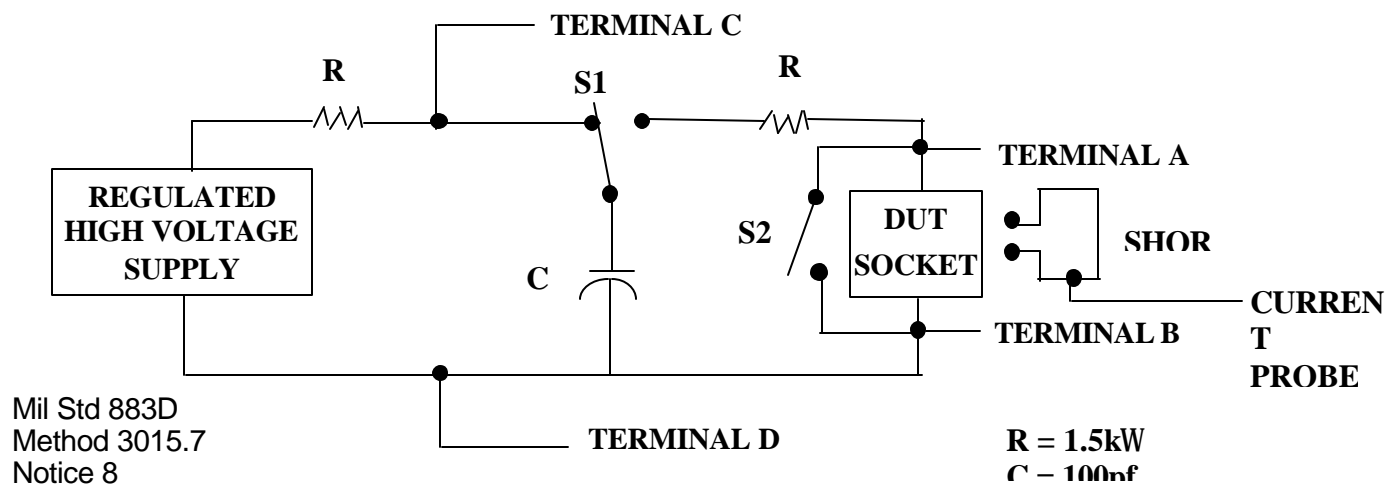
2/ No connects are not to be tested.

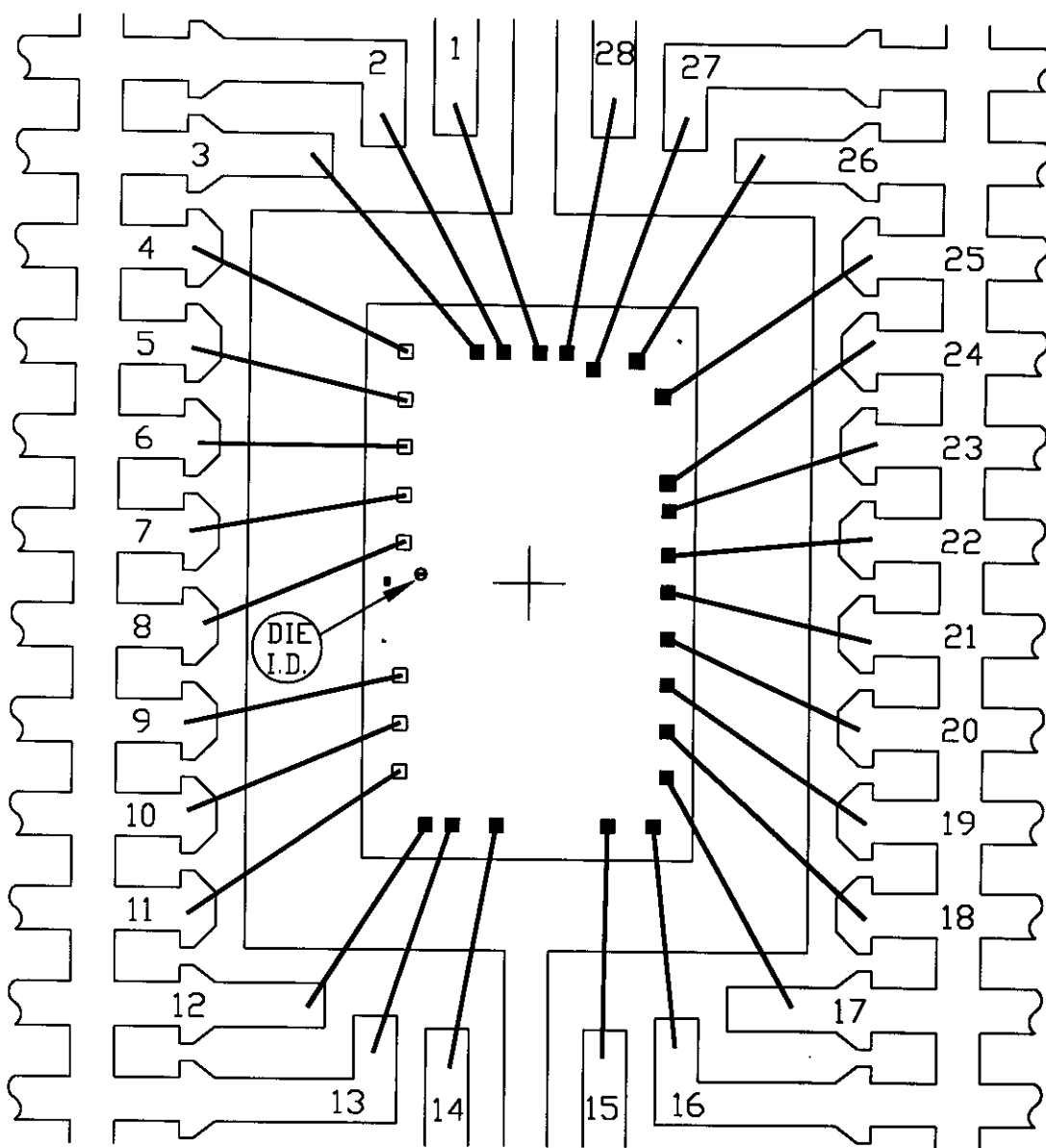
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

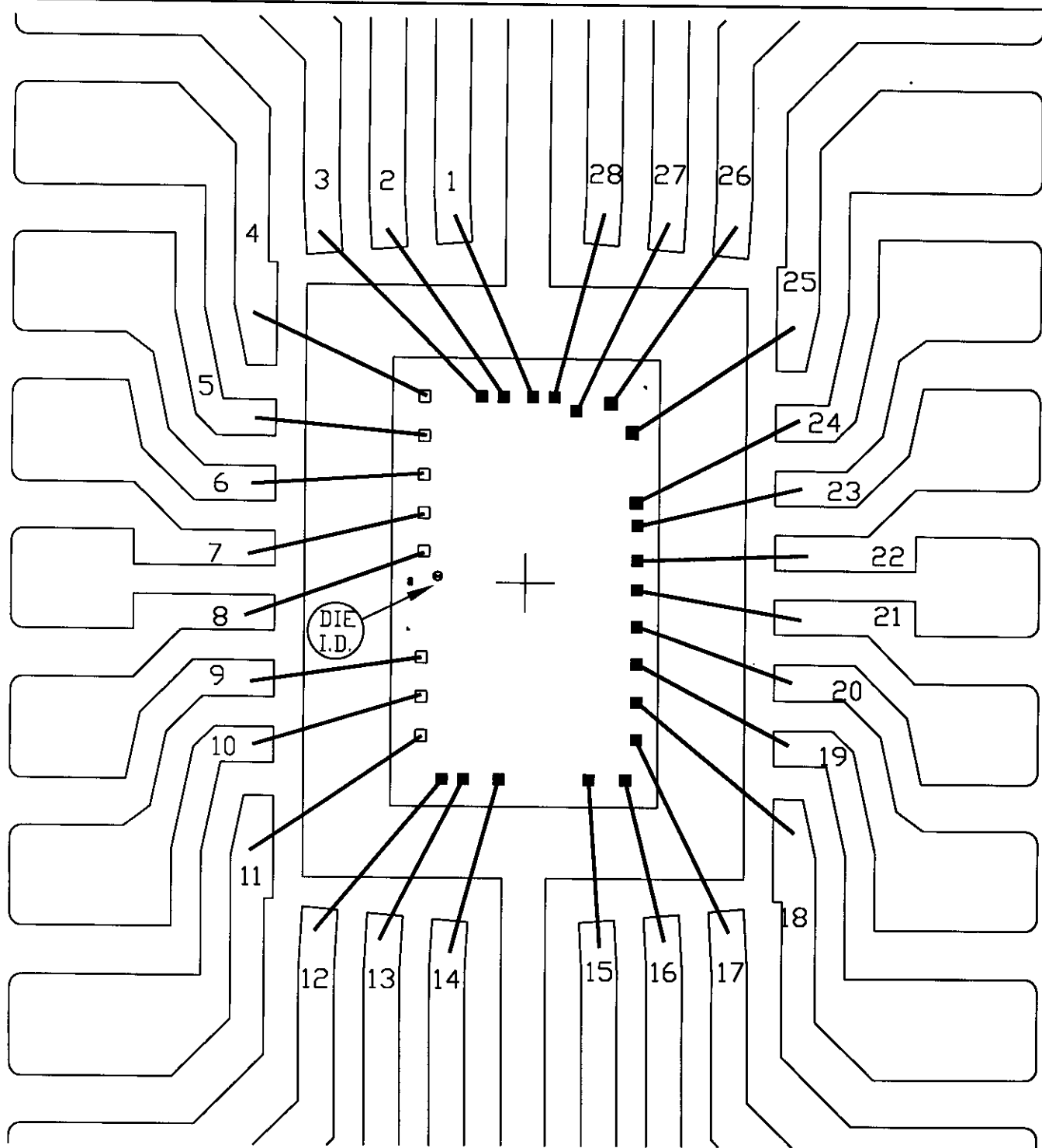
3.4 Pin combinations to be tested.

- Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

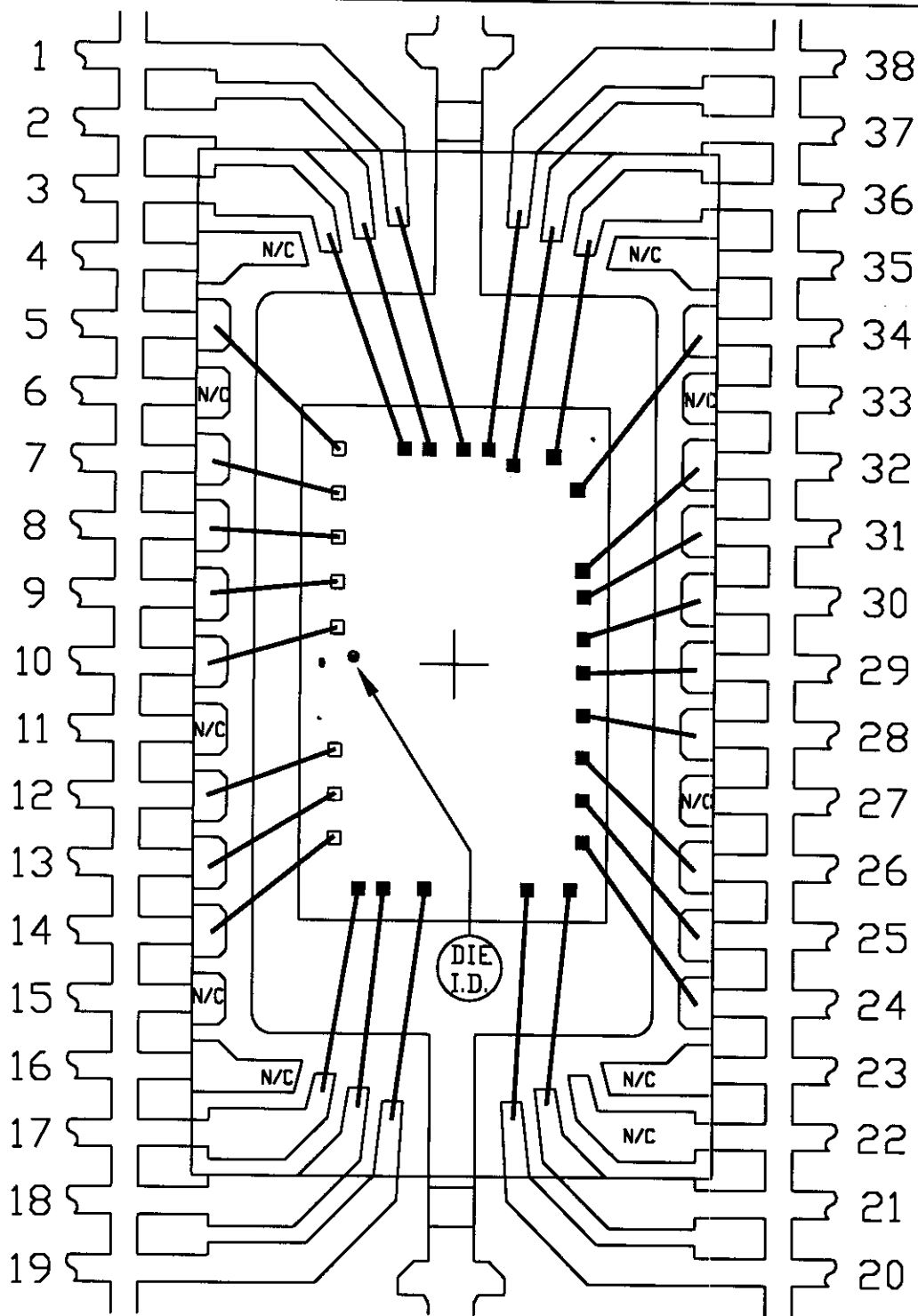




PKG.CODE: A28-1		APPROVALS	DATE	MAXIM	
CAV./PAD SIZE: 154X200	PKG. DESIGN			BUILDSHEET NUMBER: 05-1901-0053	REV.: C



PKG.CODE: W28-6		APPROVALS	DATE	MAXIM	
CAV./PAD SIZE: 150X200	PKG. DESIGN			BUILDSHEET NUMBER: 05-1901-0052	REV.: C



FOR ENGINEERING BUILD ONLY

PKG.CODE: U38-1		APPROVALS	DATE	MAXIM	
CAV./PAD SIZE: 118x217	PKG. DESIGN			BUILDSHEET NUMBER: 05-1901-0206	REV: A

