RELIABILITY REPORT

FOR

MAX3225ExxP

PLASTIC ENCAPSULATED DEVICES

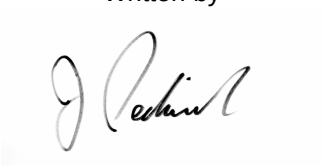
May 24, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



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Quality Assurance
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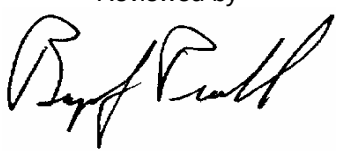


Bryan J. Preeshl
Quality Assurance
Executive Director

Conclusion

The MAX3225E successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX3225E is a 3V-powered EIA/TIA-232 and V.28/V.24 communications interface with automatic shutdown/wakeup features, high data-rate capabilities, and enhanced electrostatic discharge (ESD) protection. All transmitter outputs and receiver inputs are protected to ±15kV using IEC 1000-4-2 Air-Gap Discharge, ±8kV using IEC 1000-4-2 Contact Discharge, and ±15kV using the Human Body Model.

The MAX3225E achieves a 1µA supply current using Maxim's revolutionary AutoShutdown Plus™ feature. This device automatically enters a low-power shutdown mode when the RS-232 cable is disconnected or the transmitters of the connected peripherals are inactive, and the UART driving the transmitter inputs is inactive for more than 30 seconds. It turns on again when it senses a valid transition at any transmitter or receiver input. AutoShutdown Plus saves power without changes to the existing BIOS or operating system.

The MAX3225E also features MegaBaud™ operation, guaranteeing 1Mbps for high-speed applications such as communicating with ISDN modems. This transceiver has a proprietary low-dropout transmitter output stage enabling true RS-232 performance from a +3.0V to +5.5V supply with a dual charge pump. The charge pump requires only four small 0.1µF capacitors for operation from a 3.3V supply. The MAX3225E features a logic-level output (READY) that asserts when the charge pump is regulating and the device is ready to begin transmitting.

B. Absolute Maximum Ratings

Item	Rating
V_{CC} to GND	-0.3V to +6V
V+ to GND (Note 1)	-0.3V to +7V
V- to GND (Note 1)	+0.3V to -7V
V+ + |V-| (Note 1)	+13V
Input Voltages	
T_IN, FORCEON, /FORCEOFF to GND	-0.3V to +6V
R_IN to GND	±25V
Output Voltages	
T_OUT to GND	±13.2V
R_OUT, /INVALID, READY to GND	-0.3V to (V_{CC} + 0.3V)
Short-Circuit Duration (T_OUT to GND)	Continuous
Storage Temp.	-65°C to +160°C
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation (@70°C)	
20-Lead SSOP	640mW
20-Lead TSSOP	879mW
20-Lead PDIP	889mW
Derates above +70°C	
20-Lead SSOP	8.0mW/°C
20-Lead TSSOP	10.9mW/°C
20-Lead PDIP	11.11mW/°C

Note 1: V+ and V- can have maximum magnitudes of 7V, but their absolute difference cannot exceed 13V.

II. Manufacturing Information

A. Description/Function: ±15V ESD-Protected, 1µA, 1Mbps, 3.0V to 5.5V, RS-232 Transceiver with AutoShutdown Plus

B. Process:	S3 ((SG3) - Standard 3 micron silicon gate CMOS)
C. Number of Device Transistors:	1129
D. Fabrication Location:	Cailfornia or Oregon, USA
E. Assembly Location:	Philippines, Malyasia, Korea or Thailand
F. Date of Initial Production:	January, 1998

III. Packaging Information

A. Package Type:	**20-Lead SSOP**	**20-Lead TSSOP**	**20-Lead PDIP**
B. Lead Frame:	Copper	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-1901-0189	# 05-1901-0202	# 05-1901-0182
H. Flammability Rating:	Class UL94-V0	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1	Level 1

IV. Die Information

A. Dimensions:	91 x 159 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	3 microns (as drawn)
F. Minimum Metal Spacing:	3 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord	(Reliability Operations Manager)
Bryan Preeshl	(Executive Director of QA)
Kenneth Huening	(Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 476 \times 2}$$

(Chi square value for MTTF upper limit)

Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 2.28 \times 10^{-9}$ $\lambda = 2.28$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The attached Burn-In Schematic (#06-5402) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The RS60-4 die type has been found to have all pins able to withstand a transient pulse of ±2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Additionally, the MAX3227E has achieved ±15kV ESD protection using both methods 3015 and IEC 1000-4-2 (air-gap discharge) on the I/O pins. Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX3225ExxP

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		476	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SSOP TSSOP PDIP	77 77 77	0 0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the package.
Note 2: Generic package/process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

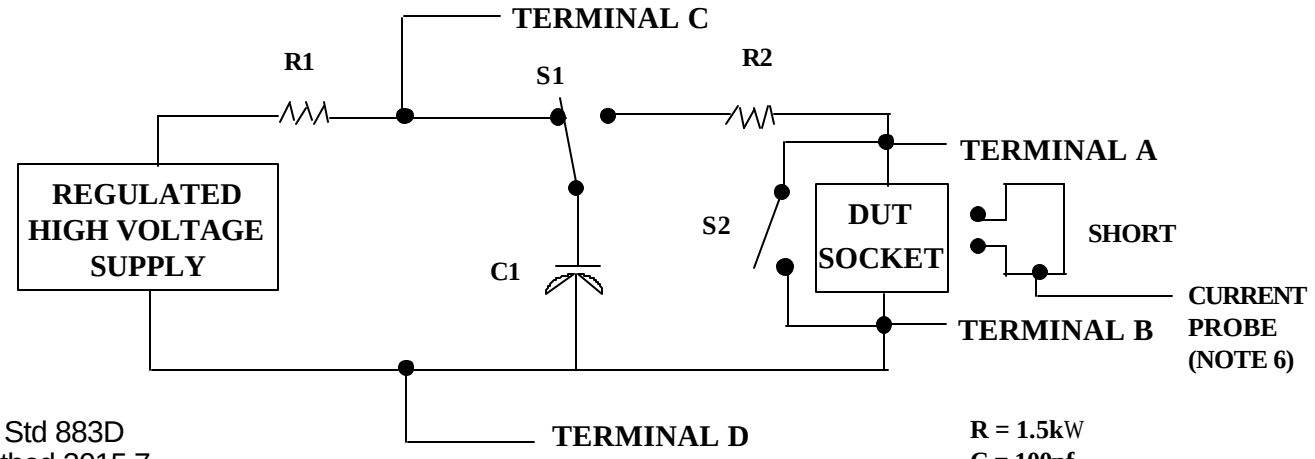
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

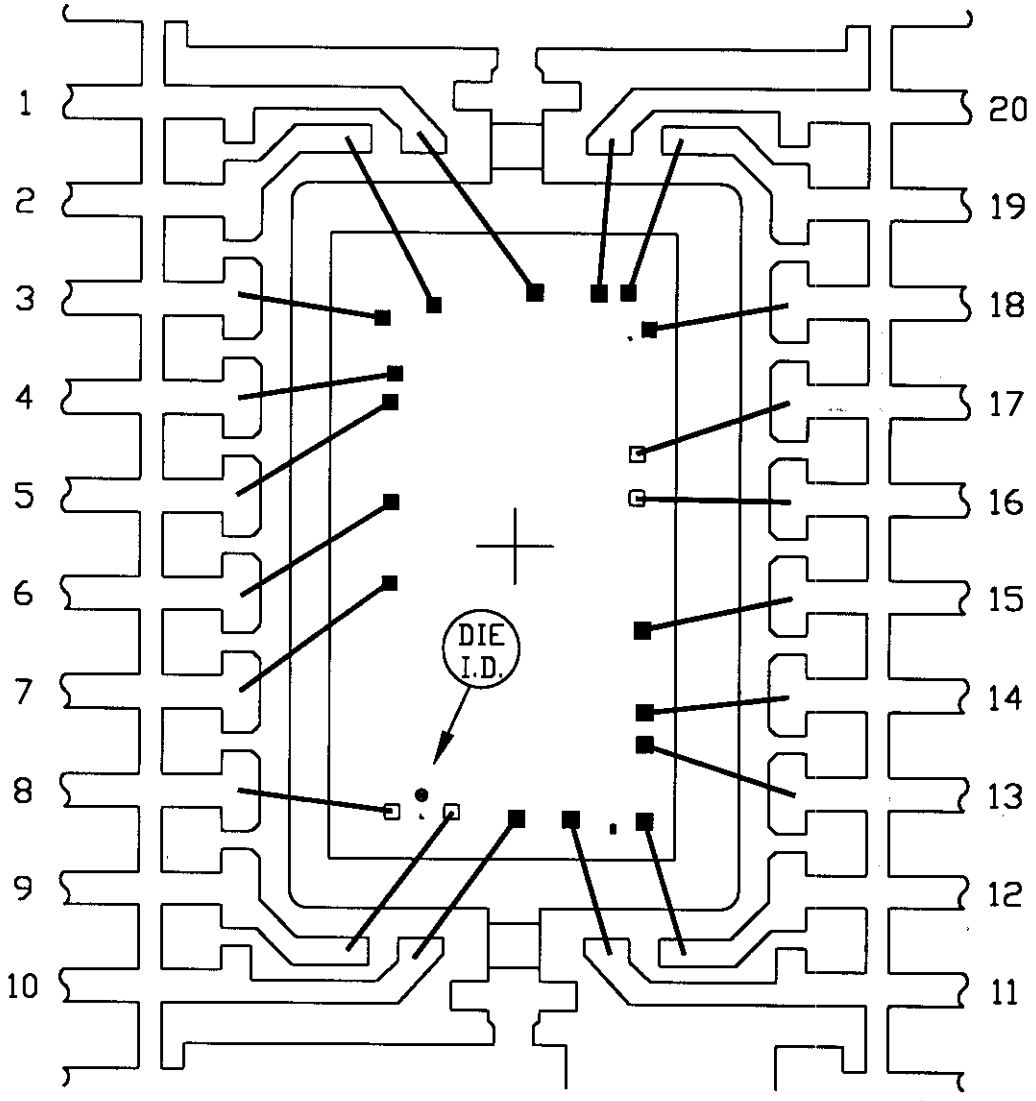
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

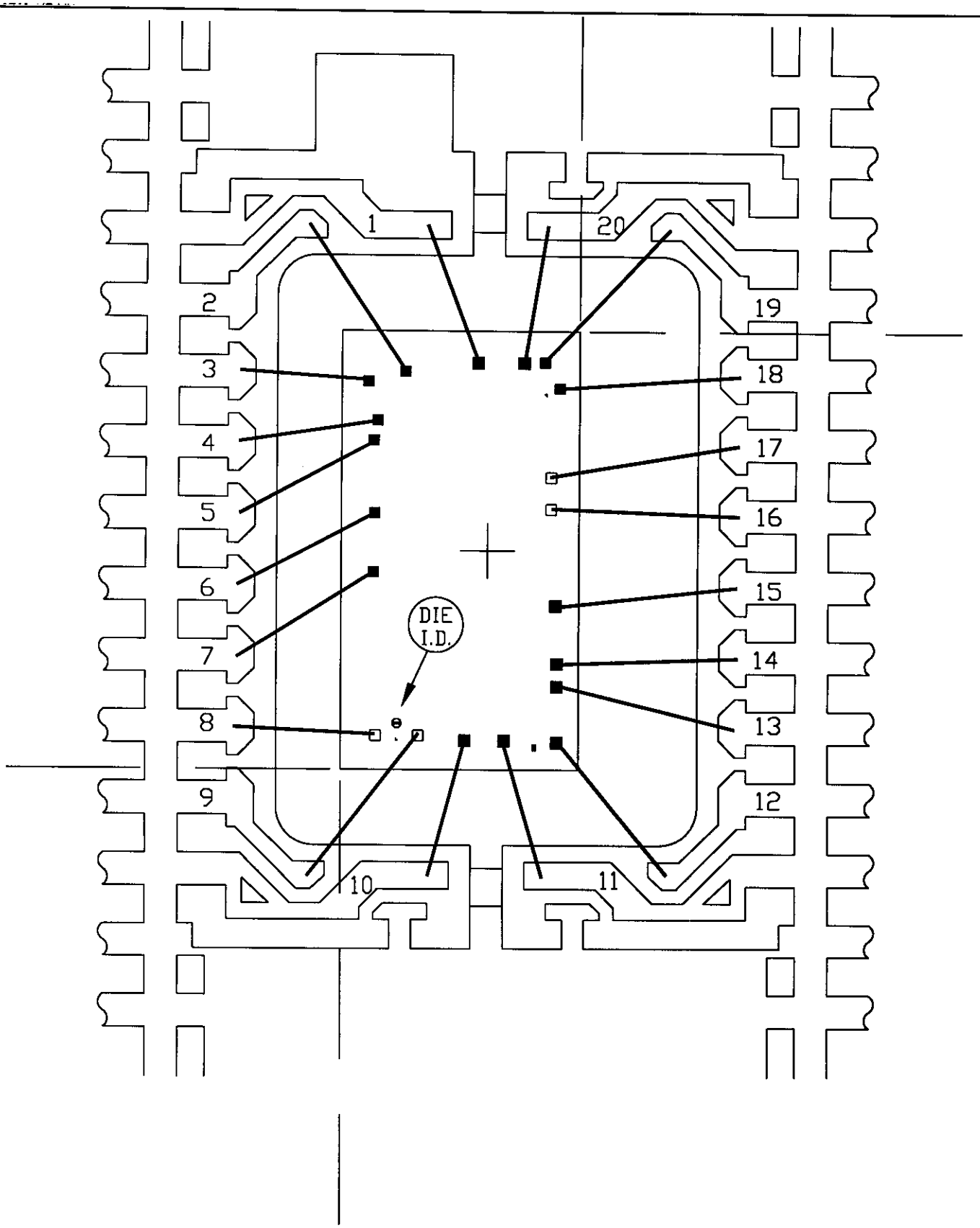
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



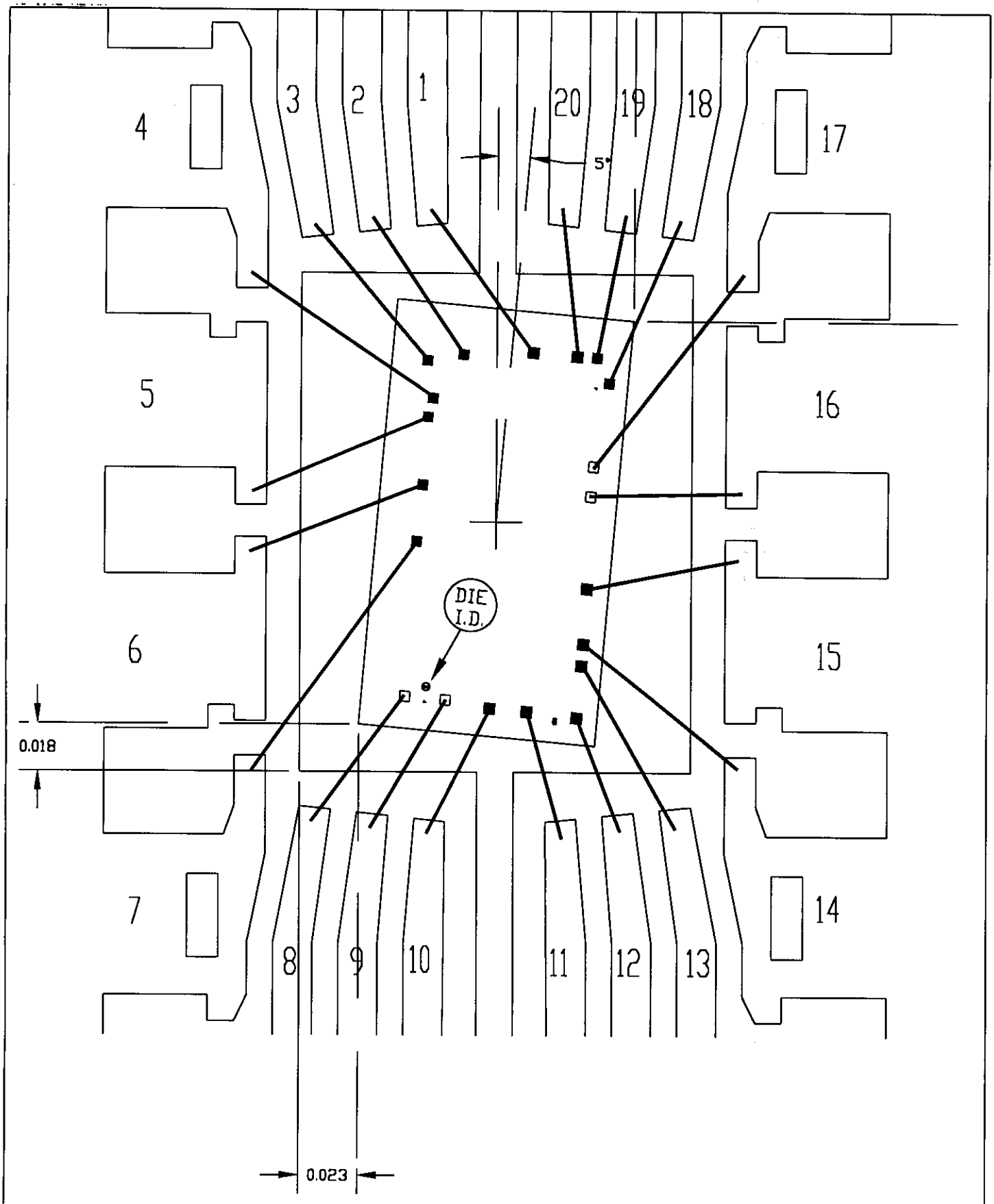
Mil Std 883D
Method 3015.7
Notice 8



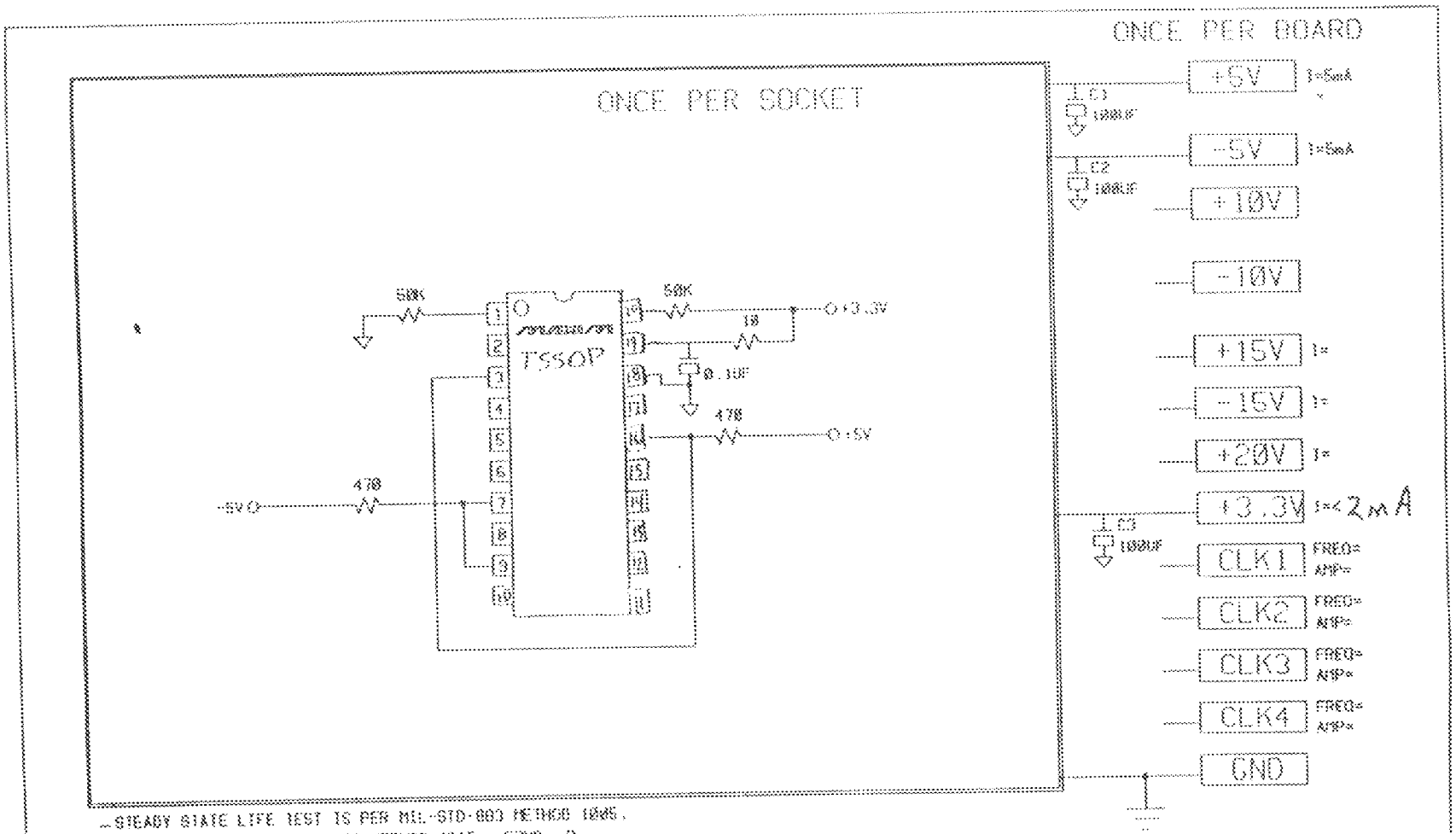
PKG.CODE: U20-2		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 118X189	PKG. DESIGN			BUILDSHEET NUMBER: 05-1901-0202 / REV.: A



PKG.CODE: A20-2		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 154X213	PKG. DESIGN			BUILDSHEET NUMBER: 05-1901-0189 / REV.: A



PKG.CODE: P20-3		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 150 X 190	PKG. DESIGN			BUILDSHEET NUMBER: 05-1901-0182 / REV.: B



...STEADY STATE LIFE TEST IS PER MIL-STD-883 METHOD 1005.
...BURN-IN IS PER MIL-STD-883 METHOD 1015, COND. D

NOTES:

1. TEMPERATURE: 125C OR EQUIVALENT
2. TIME: 168 HOURS MIN. OR EQUIVALENT
3. ALL COMPONENTS AND MATERIAL MUST STAND 150C CONTINUOUS
4. APPROVED FOR (X) COMMERCIAL
   (X) MIL/883

SPEC. NO. 06-5402 REV B

DATE: 1/19/00

DRAWN BY:

MAXIM BURN-IN SCHEMATIC

DEVICE TYPE:

MAX3222
MAX3317