### RELIABILITY REPORT

FOR

# MAX3224ExxP

PLASTIC ENCAPSULATED DEVICES

July 9, 2003

# **MAXIM INTEGRATED PRODUCTS**

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SUNNYVALE, CA 94086

Written by

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#### Conclusion

The MAX3224E successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

#### **Table of Contents**

I. ......Device Description V. ......Quality Assurance Information II. ......Manufacturing Information VI. .....Reliability Evaluation IV. .....Die Information III. ......Packaging Information .....Attachments

### I. Device Description

A. General

The MAX3224E is a 3V-powered EIA/TIA-232 and V.28/V.24 communications interface with automatic shutdown/wakeup features, high data-rate capabilities, and enhanced electrostatic discharge (ESD) protection. All transmitter outputs and receiver inputs are protected to ±15kV using IEC 1000-4-2 Air-Gap Discharge, ±8kV using IEC 1000-4-2 Contact Discharge, and ±15kV using the Human Body Model.

The device achieves a 1µA supply current using Maxim's revolutionary AutoShutdown Plus™ feature. This device automatically enter a low-power shutdown mode when the RS-232 cable is disconnected or the transmitters of the connected peripherals are inactive, and the UART driving the transmitter inputs is inactive for more than 30 seconds. They turn on again when they sense a valid transition at any transmitter or receiver input. AutoShutdown Plus saves power without changes to the existing BIOS or operating system.

The MAX3224E guarantee's 250kbps operation. The transceivers have a proprietary low-dropout transmitter output stage enabling true RS-232 performance from a +3.0V to +5.5V supply with a dual charge pump. The charge pump requires only four small 0.1µF capacitors for operation from a 3.3V supply.

The device is available in a space-saving SSOP and TSSOP packages.

### B. Absolute Maximum Ratings

<u>ltem</u>	<u>Rating</u>
VCC to GND	-0.3V to +6V
V+ to GND (Note 1)	-0.3V to +7V
V- to GND (Note 1)	+0.3V to -7V
V+ +.V(Note 1)	+13V
Input Voltages	
T_IN, FORCEON, FORCEOFF to GND	-0.3V to +6V
R_IN to GND	±25V
Output Voltages	
T_OUT to GND	±13.2V
R_OUT, INVALID, READY to GND	-0.3V to (VCC + 0.3V)
Short-Circuit Duration	
T_OUT to GND	Continuous
Operating Temperature Ranges	
MAX3224ECxx	0°C to +70°C
MAX3224EExx	-40°C to +85°C
Storage Temperature Range	-65°C to +160°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
20-Pin TSSOP	879mW
20-Pin SSOP	640mW
20-Pin PDIP	889mW
Derates above +70°C	
20-Pin TSSOP	10.09mW/°C
20-Pin SSOP	8.00mW/°C
20-Pin PDIP	11.11mW/°C

Note 1: V+ and V- can have maximum magnitudes of 7V, but their absolute difference cannot exceed 13V.

### **II.** Manufacturing Information

A. Description/Function:  $\pm 15 \text{kV}$  ESD-Protected,  $1\mu\text{A}$ , 1Mbps, 3.0V to 5.5V, RS-232 Transceivers with AutoShutdown Plus

B. Process: S3 (Standard 3 micron silicon gate CMOS)

C. Number of Device Transistors: 1129

D. Fabrication Location: Oregon, USA

E. Assembly Location: Philippines, Malaysia, Korea or Thailand

F. Date of Initial Production: January, 1998

# III. Packaging Information

A. Package Type:	20-Pin SSOP	20-Pin TSSOP	20-Pin PDIP
B. Lead Frame:	Copper	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate	Solder Plate
D. Die Attach:	Silver-Filled Epoxy	Silver-Filled Epoxy	Silver-Filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1.0 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-1901-0189	# 05-1901-0202	# 05-1901-0182
H. Flammability Rating:	Class UL94-V0	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112:	Level 1	Level 1	Level 1

### IV. Die Information

A. Dimensions: 91 x 159 mils

B. Passivation: Si<sub>3</sub>N<sub>4</sub>/SiO<sub>2</sub> (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Si (Si = 1%)

D. Backside Metallization: None

E. Minimum Metal Width: 3 microns (as drawn)

F. Minimum Metal Spacing: 3 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO<sub>2</sub>

I. Die Separation Method: Wafer Saw

### V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)

Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

# VI. Reliability Evaluation

#### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \underbrace{\frac{1}{\text{MTTF}}}_{\text{F}} = \underbrace{\frac{1.83}{192 \times 4389 \times 476 \times 2}}_{\text{Temperature Acceleration factor assuming an activation energy of } \text{Chi square value for MTTF upper limit)}$$

$$\lambda = 2.28 \times 10^{-9}$$

 $\lambda$  = 2.28 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5055) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (RR-1M).

#### B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

### C. E.S.D. and Latch-Up Testing

The RS60-3 die type has been found to have all pins able to withstand a transient pulse of  $\pm 2000 \text{V}$  per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Additionally, the MAX3222E has achieved  $\pm 15 \text{kV}$  ESD protection per method IEC 801-2 (air-gap discharge) on the I/O pins. Latch-Up testing has shown that this device withstands a current of  $\pm 250 \text{mA}$ .

# Table 1 Reliability Evaluation Test Results

# MAX3224ExxP

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test	t (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		476	0
Moisture Testi	ng (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	TSSOP SSOP PDIP	77 77 77	0 0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Str	ress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots. Note 2: Generic Package/Process data

#### Attachment #1

TABLE II. Pin combination to be tested. 1/2/

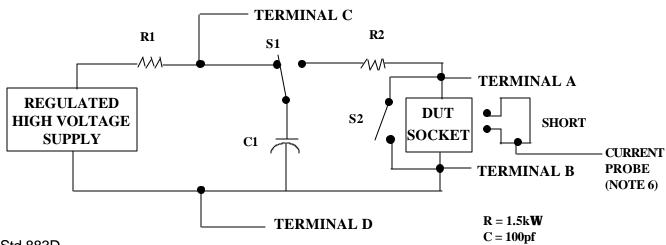
	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V <sub>PS1</sub> 3/	All V <sub>PS1</sub> pins
2.	All input and output pins	All other input-output pins

- 1/ Table II is restated in narrative form in 3.4 below.
- 2/ No connects are not to be tested.
- 3/ Repeat pin combination I for each named Power supply and for ground

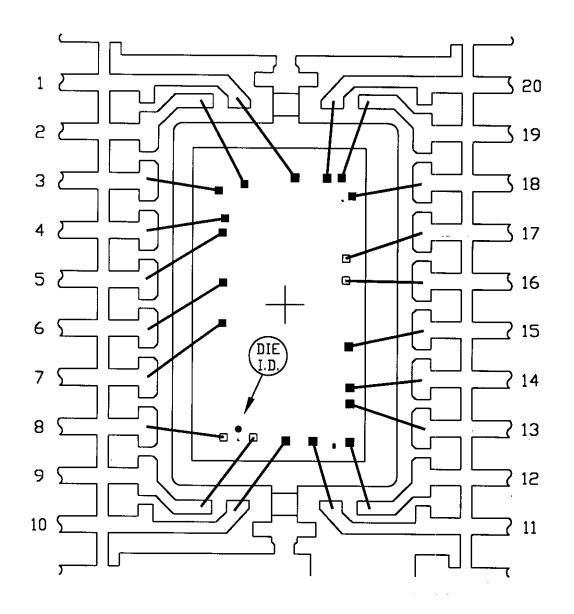
(e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ , GND,  $+V_{S}$ ,  $-V_{S}$ ,  $V_{REF}$ , etc).

# 3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g.,  $V_{SS1}$ , or  $V_{SS2}$  or  $V_{CC1}$ , or  $V_{CC2}$ ) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D Method 3015.7 Notice 8



bkecode: nso-s		APPROVALS	DATE	NINXI	<b>//</b> I
CAV./PAD SIZE:	PKG.			BUILDSHEET NUMBER:	REV.:
118X189	DESIGN			05-1901-0202	A

