RELIABILITY REPORT

FOR

MAX3170CAI

PLASTIC ENCAPSULATED DEVICES

January 23, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX3170 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX3170 is a three-driver/three-receiver multiprotocol transceiver that operates from a +3.3V single supply. The MAX3170, along with the MAX3171/MAX3173 and MAX3172/MAX3174, form a complete software-selectable data terminal equipment (DTE) or data communications equipment (DCE) interface port that supports the V.28 (RS-232), V.11 (RS-449/V.36, EIA530, EIA530-A, X.21), and V.35 protocols. The MAX3170 transceiver carries the high-speed clock and data signals, while the MAX3171 or MAX3173 carries the control signals. The MAX3170 can be terminated by the MAX3172 or MAX3174 software-selectable resistor termination network or by a discrete termination network.

An internal charge pump and proprietary low-dropout transmitter output stage allow V.11-, V.28-, and V.35-compliant operation from a +3.3V single supply. A no-cable mode is entered when all mode pins (M0, M1, and M2) are pulled high or left unconnected. In no-cable mode, supply current decreases to 1mA and all transmitter and receiver outputs are disabled (high impedance). Short-circuit limiting and thermal shutdown circuitry protect the drivers against excessive power dissipation.

B. Absolute Maximum Ratings

Item	Rating
VCC to GND	-0.3V to +4V
V+ to GND (Note 1)	-0.3V to +7V
V- to GND (Note 1)	+0.3V to –7V
V+ to V- (Note 1)	13V
M0,M1,M2,DCE/DTE, T_IN to GND	-0.3V to +6V
R_OUT to GND	-0.3V to (VCC + 0.3V)
T_OUT to GND	-15V to +15V
R_IN to GND	-15V to +15V
Storage Temp.	-65°C to +150°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	
28-Pin SSOP	889mW
Derates above +70°C	
28-Pin SSOP	11.1mW/°C

Note 1: V+ and V- can have maximum magnitudes of 7V, but their absolute difference cannot exceed 13V.

II. Manufacturing Information

A. Description/Function:	+3.3V Multiprotocol, 3 Tx/3 RX, Software-Selectable Clock/Data Transceiver
B. Process:	SG3 (Standard 3 micron silicon gate CMOS)
C. Number of Device Transistors:	4058
D. Fabrication Location:	California or Oregon, USA
E. Assembly Location:	Philippines
F. Date of Initial Production:	April, 2000

III. Packaging Information

A. Package Type:	**28-Pin SSOP**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-1901-0232
H. Flammability Rating:	Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1

IV. Die Information

A. Dimensions:	144x281 mils
B. Passivation:	SiN/SiO (nitride/oxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	3 microns (as drawn)
F. Minimum Metal Spacing:	3 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 79 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 13.75 \times 10^{-9}$

$\lambda = 13.75$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. #06-5543) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The RS86 die type has been found to have all pins able to withstand a transient pulse of ± 2500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results
MAX3170CAI

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		79	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 96hrs.	DC Parameters & functionality	SSOP	559	2
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the Small Outline package.
Note 2: Generic process/package data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

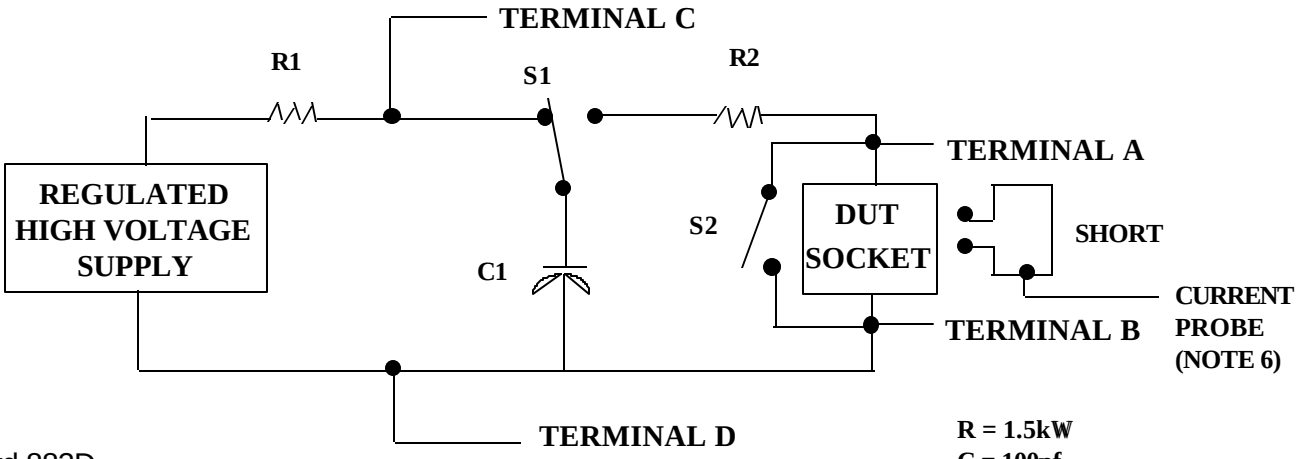
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

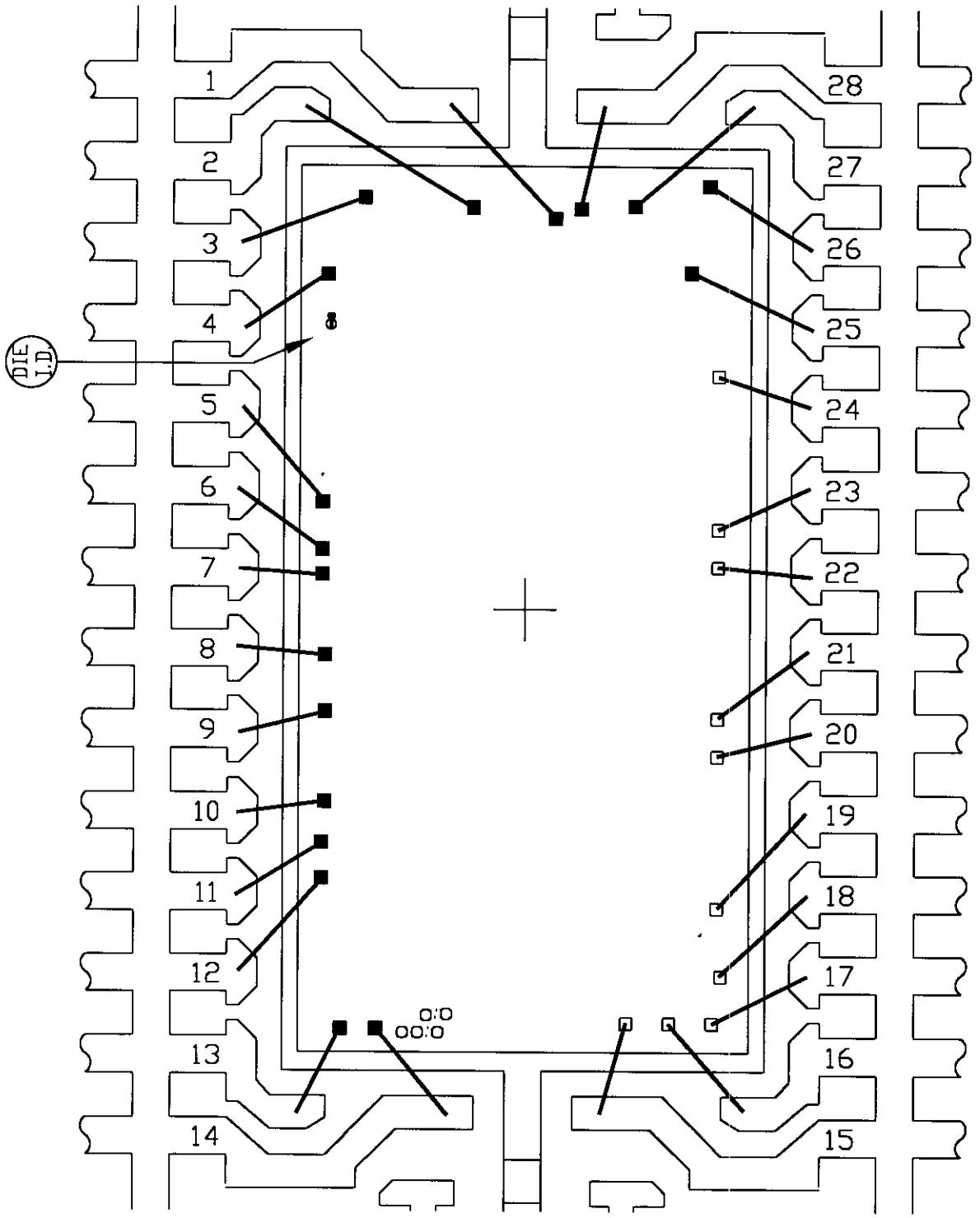
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



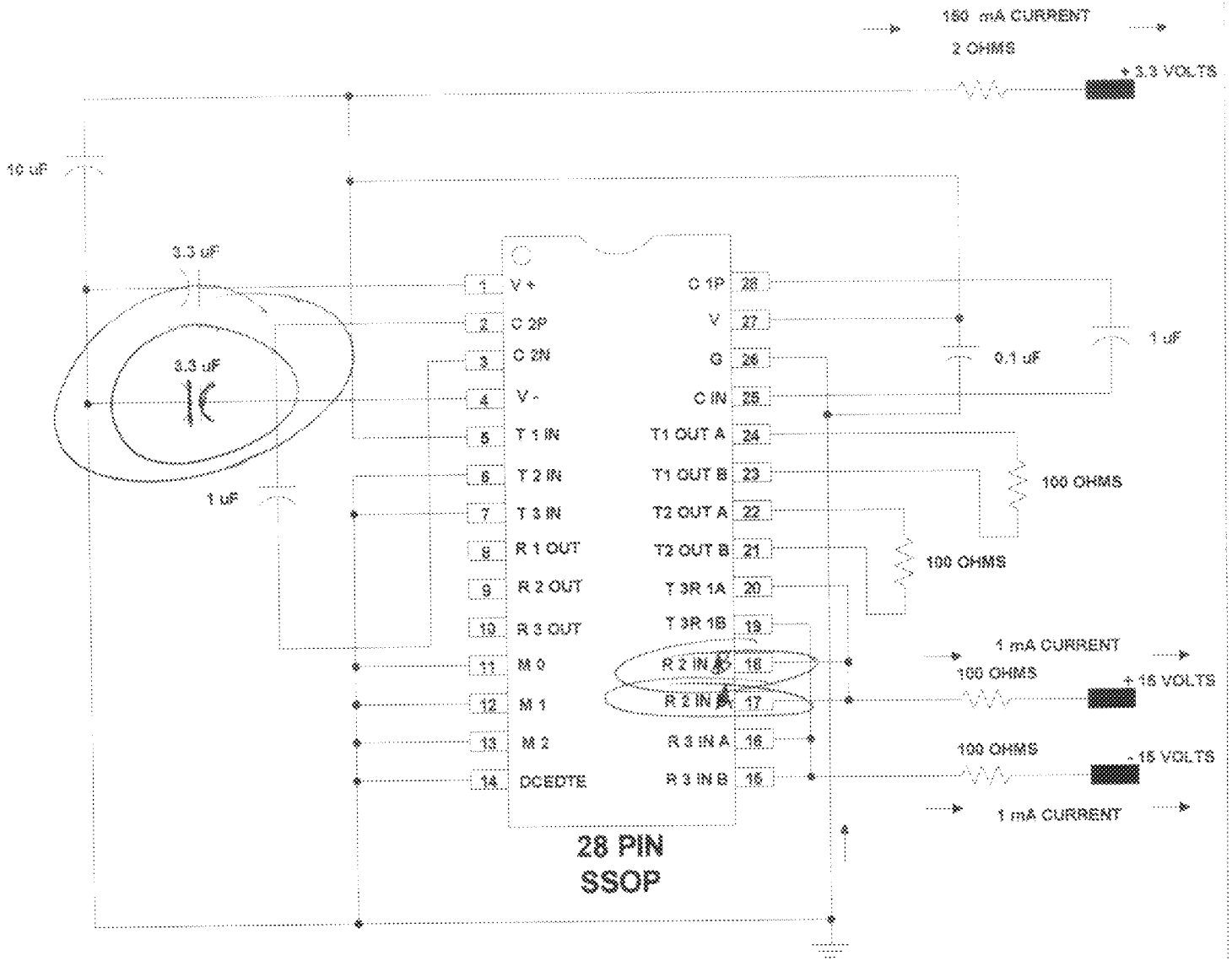
Mil Std 883D
Method 3015.7
Notice 8



PKG.CODE: A28-3		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 154X291	PKG. DESIGN			BUILDSHEET NUMBER: 05-1901-0232 / REV.: A

ONCE PER SOCKET

ONCE PER BOARD



MAXIM BURN-IN SCHEMATIC SPEC 06-5543 REV. B DATE: 3 / 7 / 2000	DEVICES: MAX 3170 / 3171 / 3173 MAX. EXPECTED CURRENT = 150 mA / 1 mA	DRAWN BY: NOTES: