MAX3088xxA Rev. A

**RELIABILITY REPORT** 

FOR

## MAX3088xxA

PLASTIC ENCAPSULATED DEVICES

February 26, 2003

# **MAXIM INTEGRATED PRODUCTS**

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## Conclusion

The MAX3088 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

#### Table of Contents

I. .....Device Description II. .....Manufacturing Information III. .....Packaging Information IV. .....Die Information V. .....Quality Assurance Information VI. .....Reliability Evaluation

.....Attachments

## I. Device Description

A. General

The MAX3088 high-speed transceiver for RS-485/RS-422 communication contains one driver and one receiver. This device features fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted. This means that the receiver output will be a logic high if all transmitters on a terminated bus are disabled (high impedance). The MAX3088's driver slew rates are not limited, making transmit speeds up to 10Mbps possible.

This transceiver typically draws 375µA of supply current when unloaded, or when fully loaded with the driver disabled.

This device has a 1/8-unit-load receiver input impedance that allows up to 256 transceivers on the bus. The MAX3088 is intended for half-duplex communications.

#### B. Absolute Maximum Ratings

ltem	Rating
Supply Voltage (V <sub>cc</sub> )	+7V
Control Input Voltage (/RE, DE)	-0.3V to (V <sub>CC</sub> + 0.3V)
Special Input Voltage	
(H//F, SRL, TXP, RXP)	-0.3V to (V <sub>CC</sub> + 0.3V)
Driver Input Voltage (DI)	-0.3V to (V <sub>cc</sub> + 0.3V)
Driver Output Voltage (A,B, Y, Z)	±13V
Reciever Input Voltage (A, B)	±13V
Reciever Input Voltage, Full Duplex (A, B)	±25V
Reciever Output Voltage (RO)	-0.3V to (V <sub>CC</sub> + 0.3V)
Storage Temp.	-65°C to +150°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	471mW
Derates above +70°C	5.88mW/°C
Continuous Power Dissipation (TA = +70°C)	
8-Pin PDIP	727mW
8-Pin SO	471mW
Derates above +70°C	
8-Pin PDIP	9.09mW/°C
8-Pin SO	5.88mW/°C

## II. Manufacturing Information

A. Description/Function: Fail-Safe, High-Speed (10Mbps), Slew-Rate-Limited RS-485/RS-422 Transceiver

B. Process:	SG3 (Standard 3 micron silicon gate CMOS)
C. Number of Device Transistors:	631
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines, Malaysia, or Thailand
F. Date of Initial Production:	March, 1997

# III. Packaging Information

A. Package Type:	8-Lead NSO	8-Lead PDIP
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	05-1901-0158	05-1901-0157
H. Flammability Rating:	Class UL94-V0	Class UL94-V0

## **IV. Die Information**

A. Dimensions:	85 x 140 mils
B. Passivation:	$Si_3N_4/SiO_2$ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	3 microns (as drawn)
F. Minimum Metal Spacing:	3 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

### V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager, Rel Operations) Bryan Preeshl (Executive Director of QA) Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

#### VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 560 \times 2}$$
(Chi square value for MTTF upper limit)  
Temperature Acceleration factor assuming an activation energy of 0.8eV  

$$\lambda = 1.94 \times 10^{-9}$$

$$\lambda = 1.94 \text{ F.I.T.}$$
 (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5188) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

#### B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

## C. E.S.D. and Latch-Up Testing

The RS46-8 die type has been found to have all pins able to withstand a transient pulse of  $\pm 2000$ V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 100$ mA.

## Table 1 Reliability Evaluation Test Results

## MAX3088xxA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test	: (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		560	0
Moisture Testir	ng (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	PDIP NSO	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Str	ess (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots. Note 2: Generic Package/Process data

# Attachment #1

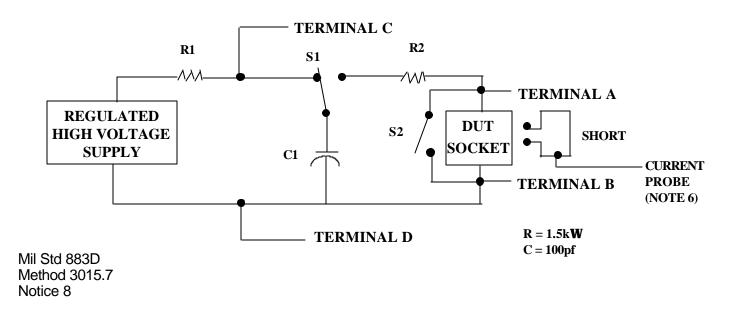
Terminal A (Each pin individually connected to terminal A with the other floating)		Terminal B (The common combination of all like-named pins connected to terminal B)		
1.	All pins except V <sub>PS1</sub> <u>3/</u>	All $V_{PS1}$ pins		
2.	All input and output pins	All other input-output pins		

TABLE II. Pin combination to be tested. 1/2/

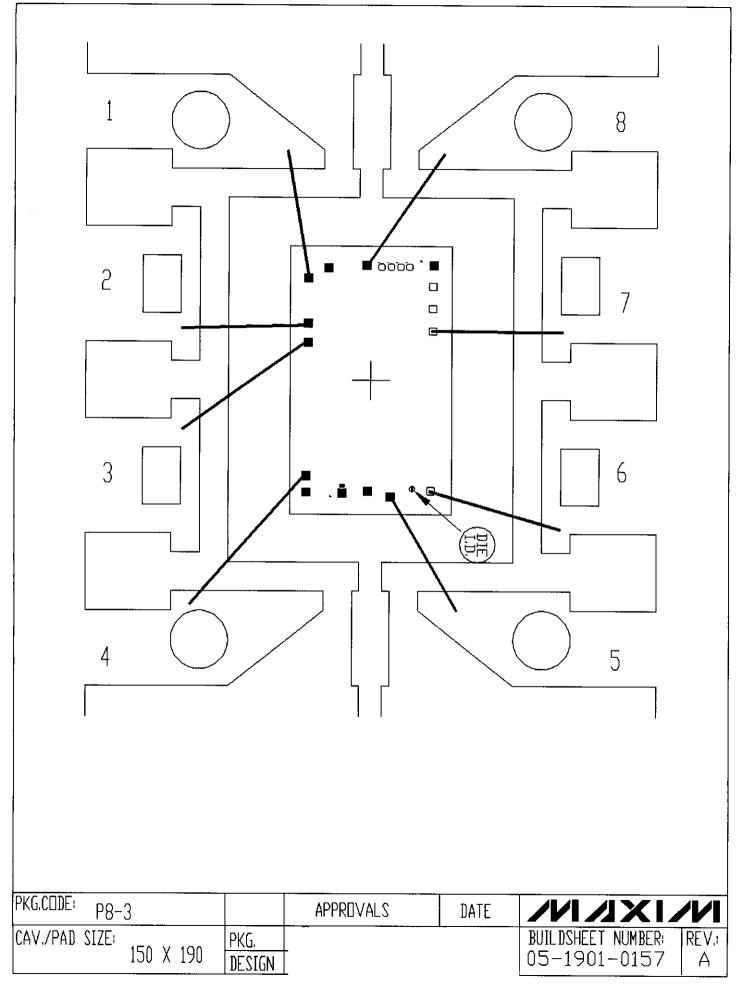
- 1/ Table II is restated in narrative form in 3.4 below.
- $\overline{2/}$  No connects are not to be tested.
- $\overline{3/}$  Repeat pin combination I for each named Power supply and for ground

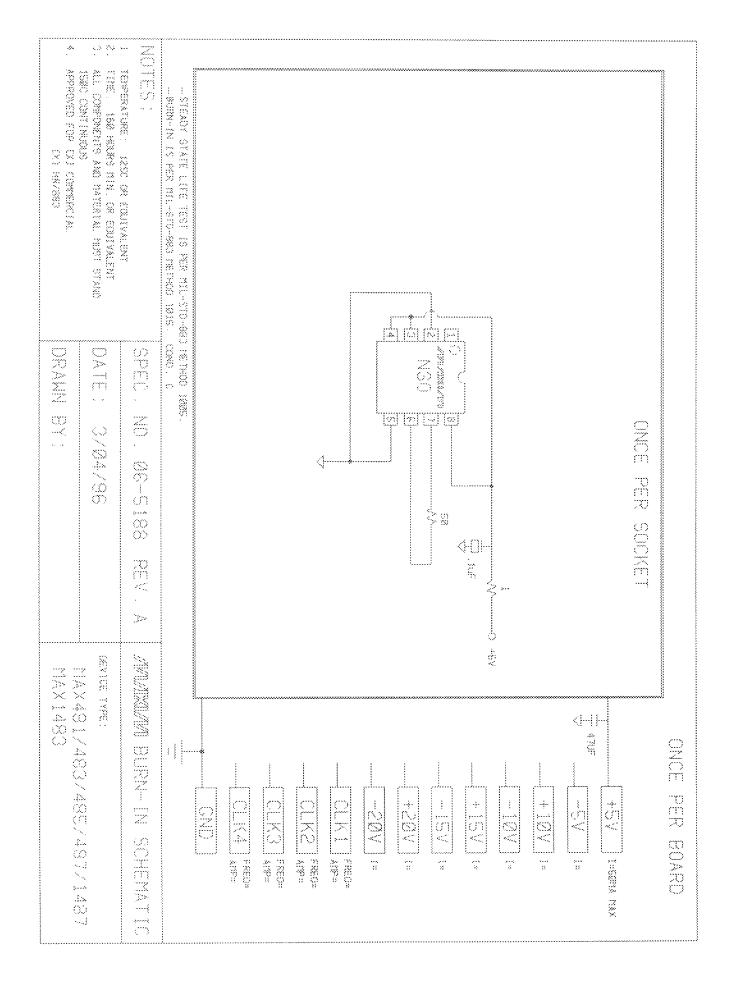
(e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ , GND, + $V_{S}$ , - $V_{S}$ ,  $V_{REF}$ , etc).

- 3.4 Pin combinations to be tested.
  - a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
  - b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V<sub>SS1</sub>, or V<sub>SS2</sub> or V<sub>SS3</sub> or V<sub>CC1</sub>, or V<sub>CC2</sub>) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
  - c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



PKG.CODE: S8-5	APPROVAL	S DATE		
CAV./PAD SIZE: 95 X 155	PKG. DESIGN		BUILDSHEET NUMBER: -05-1901-0158	REV.: A





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