

RELIABILITY REPORT
FOR
MAX2992GCB+
PLASTIC ENCAPSULATED DEVICES

June 5, 2013

MAXIM INTEGRATED

160 RIO ROBLES
SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX2992GCB+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX2992 powerline communication (PLC) baseband modem delivers half-duplex, asynchronous data communication over AC power lines at speeds up to 300kbps. The MAX2992 is a system-on-chip (SoC) that combines the physical (PHY) and media access control (MAC) layers using Maxim's 32-bit MAXQ30 microcontroller core. The MAX2991 integrated analog front-end transceiver interfaces seamlessly with the MAX2992, and together with the MAX2992 G3-PLC(tm) firmware, forms a complete G3-PLC-compliant modem solution. The MAX2992 utilizes OFDM techniques with DBPSK, DQPSK, D8PSK modulation and forward error correction (FEC) to enable robust data communication using the electrical power grid. The design provides inherent adaptability to frequency selective channels, robustness in the presence of group delay, and immunity to impulsive noise. To allow for regulatory compliance, the MAX2992 incorporates a programmable tone notching mechanism. This allows the notching of certain frequency bands in the transmit spectrum of the modem. This feature also provides an alternative method to address coexistence with other narrowband transmitters such as legacy FSK-based PLC systems. The MAX2992 MAC incorporates a 6LoWPAN adaptation layer to support IPv6 packets. An enhanced CSMA/CA and ARQ, together with the mesh routing protocol, supports all common MAC layer services for various network topologies. Intelligent communication mechanisms adapt and enhance system performance over a range of channel conditions. These mechanisms include channel estimation, adaptive tone mapping, and routing protocols. An on-chip CCM (an extension of CCM specified in IEEE® 802.15.4) authentication coprocessor with AES-128 encryption/decryption provides security and authentication.

II. Manufacturing Information

A. Description/Function:	G3-PLC MAC/PHY Powerline Transceiver
B. Process:	TS13
C. Number of Device Transistors:	2300000
D. Fabrication Location:	Taiwan
E. Assembly Location:	Korea or Taiwan
F. Date of Initial Production:	March 25, 2011

III. Packaging Information

A. Package Type:	64-pin LQFP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (0.8 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4348
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 3
J. Single Layer Theta Ja:	N/A
K. Single Layer Theta Jc:	N/A
L. Multi Layer Theta Ja:	40°C/W
M. Multi Layer Theta Jc:	8°C/W

IV. Die Information

A. Dimensions:	225.6 X 202.4 mils
B. Passivation:	SiO/SiN = 400 nm / 600 nm
C. Interconnect:	Copper
D. Backside Metallization:	None
E. Minimum Metal Width:	0.13 microns (as drawn)
F. Minimum Metal Spacing:	0.13 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

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|-----------------------------------|--|
| A. Quality Assurance Contacts: | Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA) |
| B. Outgoing Inspection Level: | 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects. |
| C. Observed Outgoing Defect Rate: | < 50 ppm |
| D. Sampling Plan: | Mil-Std-105D |

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 125C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 80 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 24.3 \times 10^{-9}$$

$$\lambda = 24.3 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

B. E.S.D. and Latch-Up Testing (lot QW5ZCQ001A, D/C 1104)

The WV20 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM:	+/- 2500V per JEDEC JESD22-A114
ESD-CDM:	+/- 750V per JEDEC JESD22-C101

Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX2992GCB+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 125°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	QW5ZCQ001A, D/C 1104

Note 1: Life Test Data may represent plastic DIP qualification lots.