

RELIABILITY REPORT
FOR
MAX293xxx
PLASTIC ENCAPSULATED DEVICES

January 30, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



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Conclusion

The MAX293 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I.Device Description	V.Quality Assurance Information
II.Manufacturing Information	VI.Reliability Evaluation
III.Packaging Information	
IV.Die InformationAttachments

I. Device Description

A. General

The MAX293 is an easy-to-use, 8th-order, lowpass, elliptic, switched-capacitor filter that can be set up with corner frequencies from 0.1Hz to 25kHz.

The MAX293's 1.5 transition ratio provides sharp rolloff and -80dB of stopband rejection. This filter has fixed responses, so the design task is limited to selecting the clock frequency that controls the filter's corner frequency.

An external capacitor is used to generate a clock using the internal oscillator, or an external clock signal can be used. An uncommitted op amp (noninverting input grounded) is provided for building a continuous-time lowpass filter for post-filtering or anti-aliasing. Steep rolloff and high order make this filter ideal for anti-aliasing applications that require maximum bandwidth and communication applications that require filtering signals in close proximity within the frequency domain.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
Supply Voltage (V+ to V-)	12V
Input Voltage at Any Pin	(V- -0.3V) V _{IN} (V+ +0.3V)
Storage Temp.	-65°C to +160°C
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation (TA = +70°C)	
16-Pin WSO	762mW
8-Pin PDIP	727mW
Derates above +70°C	
16-Pin WSO	9.52mW/°C
8-Pin PDIP	9.09mW/°C

II. Manufacturing Information

A. Description/Function:	8th-Order, Lowpass, Elliptic, Switch-Capacitor Filter
B. Process:	S3 (Standard 3 micron silicon gate CMOS)
C. Number of Device Transistors:	620
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines, Malaysia, or Thailand
F. Date of Initial Production:	May, 1992

III. Packaging Information

A. Package Type:	8-Lead PDIP	16-Lead WSO
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-0201-0111	# 05-0201-0113
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1

IV. Die Information

A. Dimensions:	89 x 95 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	3 microns (as drawn)
F. Minimum Metal Spacing:	3 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contact: Jim Pedicord (Manager, Rel Operations)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 560 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 1.94 \times 10^{-9} \quad \lambda = 1.94 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-4086) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The AF11-4 die type has been found to have all pins able to withstand a transient pulse of 1000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 200\text{mA}$.

Table 1

Reliability Evaluation Test Results

MAX293xxx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		560	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 96hrs.	DC Parameters & functionality	WSO	77	0
			PDIP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

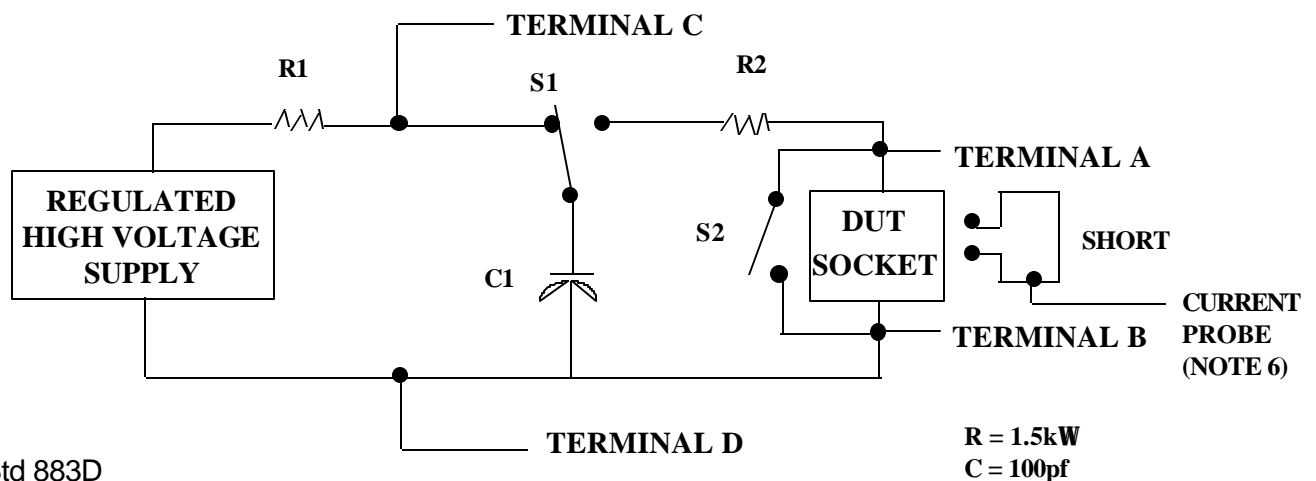
2/ No connects are not to be tested.

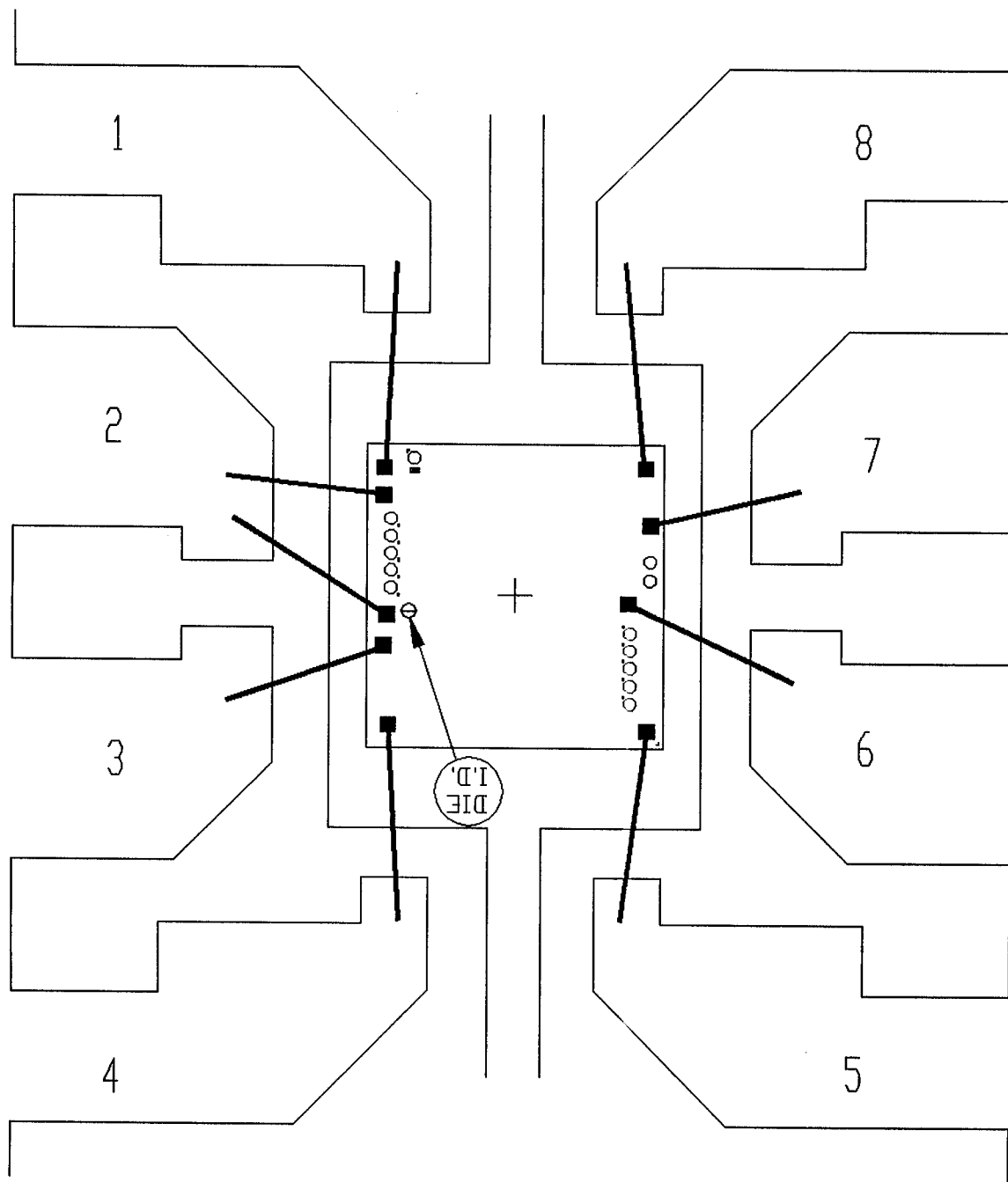
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

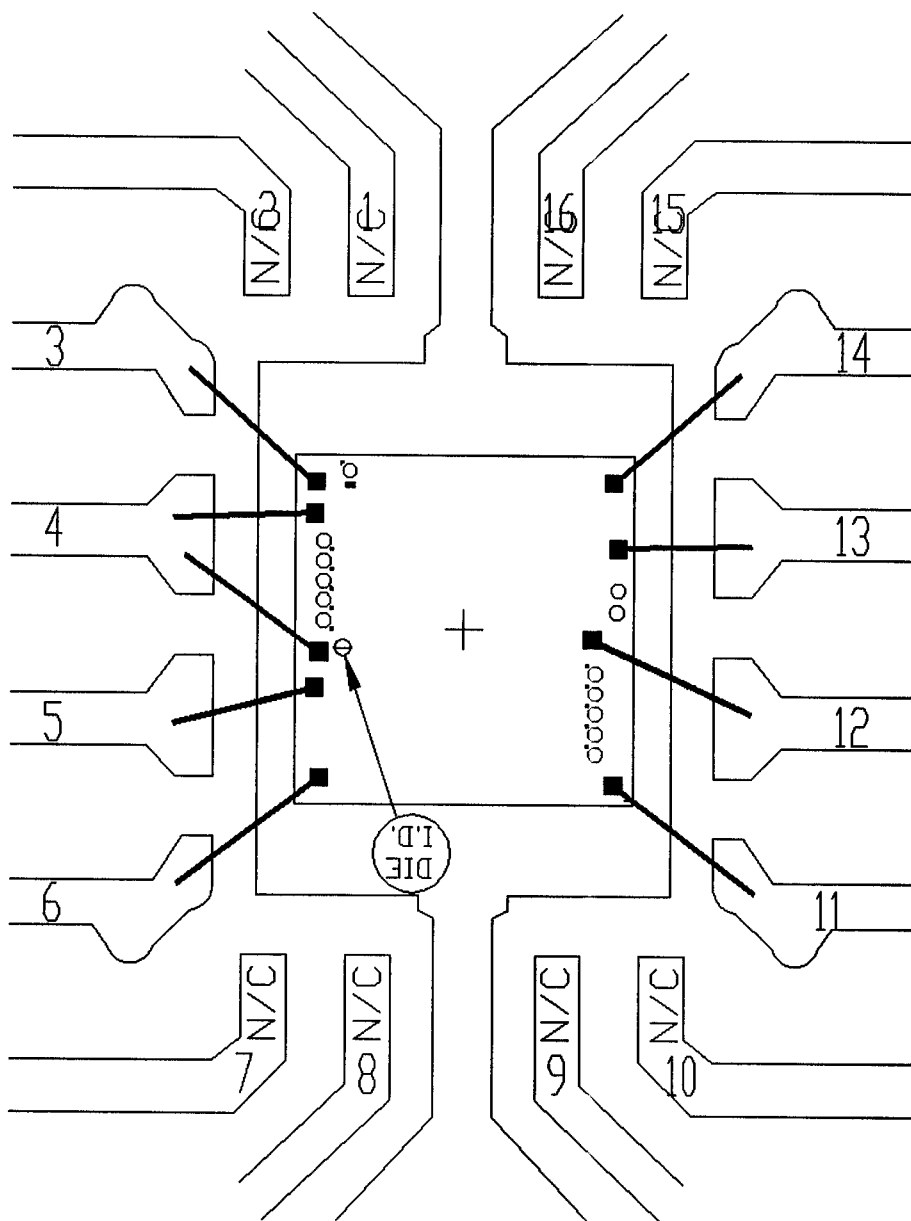
3.4 Pin combinations to be tested.

- Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.





PKG.CODE: P8-2		APPROVALS	DATE	MAXIM	
CAV./PAD SIZE: 110 X 140	PKG. DESIGN			BUILDSHEET NUMBER: 05-0201-0111	REV.: A



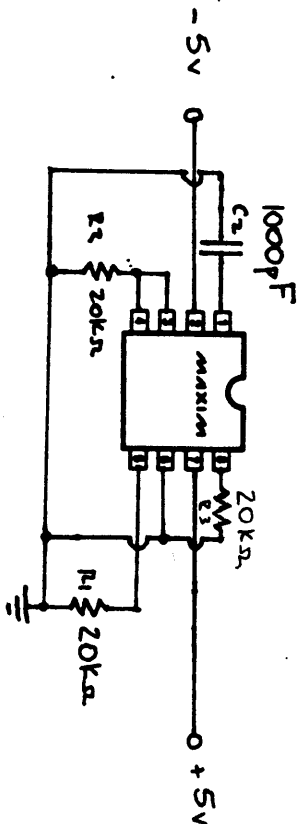
PKG. CODE: W16-1		APPROVALS	DATE	MAXIM	
CAV./PAD SIZE: 110 X 140	PKG. DESIGN			BUILDSHEET NUMBER: 05-0201-0113	REV.: A

ONCE PER SOCKET

250 Positions/Board

Top View

FUSES: ONCE/ROW



Steady state life test is per MIL-STD-883 Method 1005.

Burn-in is per MIL-STD-883 Method 1015. COND. C

- NOTES:
1. TEMPERATURE: +125 DEGREES C OR EQUIVALENT
 2. TIME: 160 HOURS MIN. OR EQUIVALENT
 3. PACKAGE TYPE:
 4. MAX. SUPPLY CURRENT PER DEVICE: $\approx 1000\mu A$, 10%, 50%
 5. C = C₁ = 0.1 uf $\pm 20\%$
 6. R₁ = R₂ = 20K Ω , 1%, 1/4W, 5%
 7. BURN-IN BOARD MATERIAL & ALL COMPONENTS MUST WITHSTAND + 150° C CONTINUOUS OPERATION.

SPEC. NO. 06-4086 REV. 0

DATE: 4/24/91

DRAWN BY:

APPROVED BY

DATE

MAXIM

BURN-IN SCHEMATIC

(AC11) MAX 291/2/3/4/5/6/7

SCALE:

ONCE PER BOARD

NOTE 4

