MAX2820ExM Rev. A

RELIABILITY REPORT

FOR

MAX2820ExM

PLASTIC ENCAPSULATED DEVICES

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MAXIM INTEGRATED PRODUCTS

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Conclusion

The MAX2820 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX2820 single-chip zero-IF transceiver is designed for the 802.11b (11Mbps) applications operating in the 2.4GHz to 2.5GHz ISM band. The MAX2820 provides a low-power shutdown mode and an analog voltage reference output feature. The transceiver includes all the circuitry required to implement an 802.11b RF-to-baseband transceiver solution, providing a fully integrated receive path, transmit path, VCO, frequency synthesis, and baseband/control interface. Only a PA, RF switch, RF BPF, and a small number of passive components are needed to form the complete radio front-end solution.

The IC eliminates the need for external IF and baseband filters by utilizing a direct-conversion radio architecture and monolithic baseband filters for both receiver and transmitter. It is specifically optimized for 802.11b (11Mbps CCK) applications. The baseband filtering and RX and TX signal paths support the CCK modulation scheme for BER = 10^{-5} at the required sensitivity levels.

The device is suitable for the full range of 802.11b data rates (1Mbps, 2Mbps, 5.5Mbps, and 11Mbps) and also the higher-rate 22Mbps PBCC[™] standard. The MAX2820 is available in the very small 7mm x 7mm 48-lead QFN package.

B. Absolute Maximum Ratings

ltem	Rating
VCC Pins to GND	-0.3V to +4.2V
RF Inputs: RX_RFP, RX_RFN to GND	-0.3V to (VCC + 0.3V)
RF Outputs: TX_RFP, TX_RFN to GND	-0.3V to +4.2V
Baseband Inputs: TX_BBIP, TX_BBIN, TX_BBQP,	
TX_BBQN to GND	-0.3V to (VCC + 0.3V)
Baseband Outputs: RX_BBIP, RX_BBIN, RX_BBQP,	
RX_BBQN to GND	-0.3V to (VCC + 0.3V)
Analog Inputs: RX_AGC, TX_GC, TUNE, ROSCN,	
ROSCP to GND	-0.3V to (VCC + 0.3V)
Analog Outputs: PA_BIAS, CP_OUT, VREF to GND	-0.3V to (VCC + 0.3V)
Digital Inputs: RX_ON, TX_ON, SHDNB, CSB, SCLK,	
DIN, RF_GAIN, RX_1K to GND	-0.3V to (VCC + 0.3V)
Bias Voltages: RBIAS, BYP	+0.9V to +1.5V
Short-Circuit Duration Digital Outputs: DOUT, RX_DET	10s
RF Input Power: RX_RFN, RX_RFP	+10dBm
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +160°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
48-Pin QFN	2162mW
48-Pin Thin QFN	3077mW
Derates above +70°C	
48-Pin QFN	27.0mW/°C
48-Pin Thin QFN	38.5mW/°C

II. Manufacturing Information

A. Description/Function:	2.4GHz 802.11b Zero-IF Transceivers
B. Process:	GST4
C. Number of Device Transistors:	13,607
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Korea or Hong Kong
F. Date of Initial Production:	January, 2003

III. Packaging Information

A. Package Type:	48-Pin Thin QFN (7 x 7)	48-Pin QFN (7 x 7)
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled epoxy	Silver-filled epoxy
E. Bondwire:	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-9000-0097	Buildsheet # 05-7001-0564
H. Flammability Rating:	Class: UL94-V0	Class: UL94-V0
 Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: 	Level 1	Level 3

IV. Die Information

A. Dimensions:	142 x 166 mils
B. Passivation:	Si ₃ N ₄ (Silicon nitride)
C. Interconnect:	Au
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1: 1.2; Metal2: 1.2; Metal3: 1.2; Metal4: 5.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1: 1.6; Metal2: 1.6; Metal3: 1.6; Metal4: 4.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

Α.	Quality Assurance Contacts:	Jim Pedicord	(Manager, Reliability Operations)
		Bryan Preeshl	(Executive Director of QA)
		Kenneth Huening	(Vice President)

- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

 $\lambda = \underbrace{1}_{\text{MTTF}} = \underbrace{1.83}_{192 \text{ x } 9823 \text{ x } 90 \text{ x } 2} \text{ (Chi square value for MTTF upper limit)}_{\text{L}}$ Temperature Acceleration factor assuming an activation energy of 0.8eV

 $\lambda = 5.39 \text{ x } 10^{-8}$ $\lambda = 5.39 \text{ F.I.T.}$ (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The Burn-In Schematic (Spec.# 06-7021) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Reports (**RR-1M & RR-B3A**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The WD05-1 die type has been found to have all pins able to withstand a transient pulse of +/-200V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ± 250 mA.

Table 1Reliability Evaluation Test Results

MAX2820ExM

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Tes	t (Note 1)			
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality	90	0
Moisture Testi	ng (Note 2)			
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Str	ress (Note 2)			
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic process/package data.

Attachment #1

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V _{PS1} <u>3/</u>	All V _{PS1} pins
2.	All input and output pins	All other input-output pins

TABLE II. Pin combination to be tested. 1/2/

- 1/ Table II is restated in narrative form in 3.4 below.
- $\frac{2}{3}$ No connects are not to be tested. 3/ Repeat pin combination I for each
- $\overline{3/}$ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_{S}$, $-V_{S}$, V_{REF} , etc).

3.4 <u>Pin combinations to be tested.</u>

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.









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