

RELIABILITY REPORT

FOR

MAX2769BETI/V+

PLASTIC ENCAPSULATED DEVICES

July 15, 2011

# **MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR. SUNNYVALE, CA 94086

Approved by			
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#### Conclusion

The MAX2769BETI/V+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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#### I. Device Description

#### A. General

The MAX2769B is a next-generation Global Navigation Satellite System (GNSS) receiver covering GPS, GLONASS, Galileo, and Compass navigation satellite systems on a single chip. This single-conversion GNSS receiver is designed to provide high performance for industrial and automotive applications. Designed on Maxim's advanced, low-power SiGe BiCMOS process technology, the MAX2769B offers the highest performance and integration at a low cost. Incorporated on the chip is the complete receiver chain, including a dual-input LNA and mixer, followed by the image-rejected filter, PGA, VCO, fractional-N frequency synthesizer, crystal oscillator, and a multibit ADC. The total cascaded noise figure of this receiver is as low as 1.4dB. The MAX2769B completely eliminates the need for external IF filters by implementing on-chip monolithic filters and requires only a few external components to form a complete low-cost GPS RF receiver solution. The MAX2769B is the most flexible receiver on the market. The integrated delta-sigma fractional-N frequency synthesizer allows programming of the IF frequency within a ±30Hz (fXTAL = 32MHz) accuracy while operating with any reference or crystal frequencies that are available in the host system. The ADC outputs CMOS logic levels with 1 or 2 quantized bits for both I and Q channels, or up to 3 quantized bits for the I channel. I and Q analog outputs are also available. The MAX2769B is packaged in a 5mm x 5mm, 28-pin thin QFN package with an exposed paddle.



#### II. Manufacturing Information

A. Description/Function: Universal GPS Receiver

B. Process: MB3C. Number of Device Transistors: 68846D. Fabrication Location: California

E. Assembly Location: China and TaiwanF. Date of Initial Production: June 2, 2011

## III. Packaging Information

A. Package Type: 28-pin TQFN 5x5

B. Lead Frame: Copper

C. Lead Finish: 100% matte Tin
D. Die Attach: Conductive
E. Bondwire: Au (1 mil dia.)

F. Mold Material: Epoxy with silica filler
 G. Assembly Diagram: #05-9000-4494
 H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per Level 1

JEDEC standard J-STD-020-C

J. Single Layer Theta Ja: 47°C/W
K. Single Layer Theta Jc: 2.1°C/W
L. Multi Layer Theta Ja: 29°C/W
M. Multi Layer Theta Jc: 2.1°C/W

#### IV. Die Information

A. Dimensions: 91.73X84.65 mils

B. Passivation: BCB

C. Interconnect: All with top layer 100% Cu

D. Backside Metallization: NoneE. Minimum Metal Width: 0.35μmF. Minimum Metal Spacing: 0.35μm

G. Bondpad Dimensions:

H. Isolation Dielectric: SiO<sub>2</sub>I. Die Separation Method: Wafer Saw



#### V. Quality Assurance Information

A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)

Don Lipps (Manager, Reliability Engineering)

Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm</li>D. Sampling Plan: Mil-Std-105D

#### VI. Reliability Evaluation

#### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( 3) is calculated as follows:

$$x = 22.9 \times 10^{-9}$$

x = 22.9 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the MB3 Process results in a FIT Rate of 0.08 @ 25C and 1.33 @ 55C (0.8 eV, 60% UCL)

## B. E.S.D. and Latch-Up Testing (lot SS70BQ001C, D/C 1106)

The WV10 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.



# **Table 1**Reliability Evaluation Test Results

# MAX2769BETI/V+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (No	ote 1) Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	SS70BQ001C, D/C 1106

Note 1: Life Test Data may represent plastic DIP qualification lots.