MAX2754EUA Rev. A

RELIABILITY REPORT

FOR

MAX2754EUA

PLASTIC ENCAPSULATED DEVICES

September 9, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Reviewed by

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Conclusion

The MAX2754 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX2754 self-contained, linear modulation, voltage-controlled oscillator (VCO) is intended for use in the 2.4GHz to 2.5GHz ISM band, particularly for FSK modulation systems that utilize a direct frequency-modulation transmit architecture. This device features a linear modulation input in addition to the standard frequency tuning input. The frequency tuning range of 1145MHz to 1250MHz (1/2 LO) also supports an IF up to 110MHz with low side LO. The VCO is based on Maxim's proprietary monolithic VCO technology, where all VCO components are integrated on-chip, including the varactor and inductor.

The MAX2754 linear modulation input offers a means to directly FM modulate the VCO with a constant modulation sensitivity over the tuning voltage input range. Typical frequency deviation is -500kHz/V which is linear to $\pm 4\%$ over the guaranteed frequency limits. The tuning input voltage range is +0.4V to +2.4V and the oscillator frequency is factory adjusted to provide guaranteed limits. The oscillator signal is buffered by an output amplifier stage (internally matched to 50 Ω) to provide higher output power and isolate the oscillator from load impedance variations.

The MAX2754 operates over a +2.7V to +5.5V supply range. This device also provides a digitally controlled shutdown mode to permit implementation of sophisticated power-supply management. In shutdown, the supply current is reduced to 0.2μ A. Even when active, power consumption is a modest 41mW.

The MAX2754 is packaged in the miniature 8-pin μ MAX to offer the world's smallest, complete 2.4GHz direct-modulation VCO solution.

B. Absolute Maximum Ratings

Rating
-0.3V to +6.0V
-0.3V to +6.0V
-0.3V to (VCC + 0.3V)
-0.3V to +6.0V
-40°C to +85°C
+150°C
-65°C to +160°C
+300°C
457mW
5.7mW/°C

II. Manufacturing Information

A. Description/Function:	1.2GHz VCO with Linear Modulation Input
B. Process:	MB14 Bi-CMOS Process
C. Number of Device Transistors:	619
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Korea
F. Date of Initial Production:	July, 2001

III. Packaging Information

A. Package Type:	8-Pin µMAX
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-Filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-3101-0002
H. Flammability Rating:	Class UL94-V0
 Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: 	Level 1

IV. Die Information

A. Dimensions:	73 x 59 mils
B. Passivation:	Si ₃ N ₄ (Silicon nitride)
C. Interconnect:	Au
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn) Metal 1&2, 2.8 microns (as drawn) Metal 3
F. Minimum Metal Spacing:	1.6 microns (as drawn) Metal 1&2, 2.8 microns (as drawn) Metal 3
G. Bondpad Dimensions:	3 mil. Octagonal
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

Α.	Quality Assurance Contacts:	Jim Pedicord	(Manager, Reliability Operations)
		Bryan Preeshl	(Executive Director of QA)
		Kenneth Huening (Vice President)	

- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

 $\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 9823 \times 45 \times 2}$ (Chi square value for MTTF upper limit) Temperature Acceleration factor assuming an activation energy of 0.8eV $\lambda = 10.78 \times 10^{-9}$ $\lambda = 10.78 \text{ F.I.T.}$ (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic #06-5849 shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The WD03 die type has been found to have all pins able to withstand a transient pulse of \pm 600V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit).

Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1Reliability Evaluation Test Results

MAX2754EUA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Tes	t (Note 1)			
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality	45	0
Moisture Testi	ng (Note 2)			
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots. Note 2: Generic package/process data.

Attachment #1

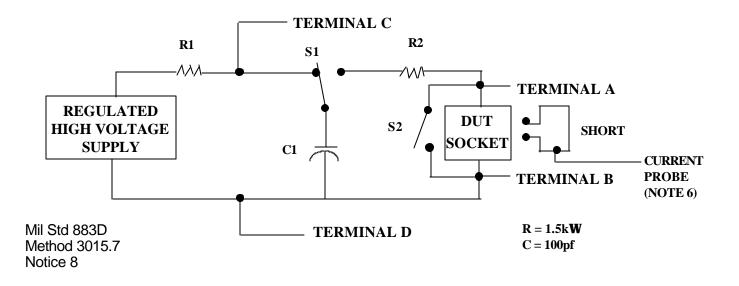
	TABLE II.	Pin combination to be tested.	1/ 2/
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	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V _{PS1} <u>3/</u>	All V _{PS1} pins
2.	All input and output pins	All other input-output pins

- 1/ Table II is restated in narrative form in 3.4 below.
- $\overline{2}$ / No connects are not to be tested.
- $\overline{\underline{3}}$ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_{S}$, $-V_{S}$, V_{REF} , etc).

- 3.4 <u>Pin combinations to be tested.</u>
 - a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
 - b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
 - c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



PKG. CODE: U8-1 CAV./PAD SIZE: 68×94	SIGNATURES DATE PKG. DESIGN	CONFIDENTIAL & PROPRIETARY BOND DIAGRAM #: REV: 05-3101-0002 A

