RELIABILITY REPORT

FOR

MAX2679BENS+T

WAFER LEVEL DEVICES

May 7, 2017

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

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Conclusion

The MAX2679BENS+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX2679 and MAX2679B low-noise amplifiers (LNA) are designed for GPS L1, Galileo, and GLONASS applications. The devices achieve high gain and low noise figure while maximizing the input-referred 1dB compression point and the 3rd-order intercept point. The MAX2679 achieves excellent performance while consuming only 1mA supply current and providing 0.95dB noise figure. The MAX2679B achieves excellent performance while consuming only 650ìA and providing 1.03dB noise figure. The MAX2679/MAX2679B operates from a +1.08V to +1.98V single supply. The devices are available in a very small, lead-free, RoHS-compliant, 0.83mm x 0.83mm wafer-level package (WLP).

II. Manufacturing Information

A. Description/Function:	GPS/GNSS Ultra-Low Current Low-Noise Amplifier
B. Process:	SBC18
C. Fabrication Location:	USA
D. Assembly Location:	Taiwan
E. Date of Initial Production:	March 21, 2017

III. Packaging Information

A. Package Type:	4-bump thin WLP
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	None
E. Bondwire:	N/A (N/A mil dia.)
F. Mold Material:	None
G. Assembly Diagram:	#05-100365
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	N/A°C/W
K. Single Layer Theta Jc:	N/A°C/W
L. Multi Layer Theta Ja:	102.59°C/W
M. Multi Layer Theta Jc:	N/A°C/W

IV. Die Information

A. Dimensions:	33.8583X33.8583 mils
B. Passivation:	Si_3N_4/SiO_2
C. Interconnect:	Al with Ti/TiN Barrier
D. Minimum Metal Width:	0.23 microns (as drawn)
E. Minimum Metal Spacing:	0.23 microns (as drawn)
F. Isolation Dielectric:	SiO_2
G. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Eric Wright (Reliability Engineering) Brian Standley (Manager, Reliability) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{1000 \times 4340 \times 240 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 0.88 \times 10^{-9}$

$\lambda = 0.88$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the SBC18 Process results in a FIT Rate of 0.04@ 25C and 0.69@ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The RH16-0 die type has been found to have all pins able to withstand an HBM transient pulse of +/-1500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX2679BENS+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C Biased Time = 1000 hrs.	DC Parameters & functionality	240	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.