RELIABILITY REPORT

FOR

MAX2670GTB+

PLASTIC ENCAPSULATED DEVICES

November 21, 2014

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX2670GTB+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX2670 GPS/GNSS front-end amplifier IC is designed for automotive and marine GPS/GNSS satellite navigation antenna modules or for any application that needs to compensate for cable losses from the antenna to receiver. Two unconditionally stable low-noise amplifier stages provide the high gain and integrated I/O matching to minimize the need for external matching components and eliminate the need for additional gain stages. The device features the option to place a bandpass ceramic or SAW filter between the two amplifier stages to provide a narrow-band output to further improve the noise performance of the GPS/GNSS receiver. Additionally, a 3.4dB gain step is provided to compensate for cable loss variation between different applications. The device is designed to operate across all GNSS frequency standards with a 34.8dB typical cascaded gain and a 25mA supply current. The two LNA stages allow the use of a wide range of GNSS filter types for maximum flexibility in system design. The final RF output pin, which drives the cable to the GNSS receiver, is also the power-supply connection that accepts a DC supply in the +3.0V to +5.5V range. Alternatively, the DC supply can be applied to pin 4. This GPS/GNSS front-end amplifier is designed on a low-noise, advanced SiGe process and is available in a lead-free, 10-pin TDFN surface-mount package (3mm x 3mm).

II. Manufacturing Information

A. Description/Function:	GPS/GNSS Front-End Amplifier
B. Process:	G4
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon
E. Assembly Location:	Taiwan, China, Thailand, Malaysia
F. Date of Initial Production:	June 23, 2011

III. Packaging Information

A. Package Type:	10-pin TDFN 3x3
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-1967
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	54°C/W
K. Single Layer Theta Jc:	8.5°C/W
L. Multi Layer Theta Ja:	41°C/W
M. Multi Layer Theta Jc:	8.5°C/W

IV. Die Information

A. Dimensions:	58X49 mils
B. Passivation:	Si_3N_4
C. Interconnect:	Au
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn) Metal 1, 2 & 3
F. Minimum Metal Spacing:	1.6 microns (as drawn) Metal 1, 2 & 3
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{1000 \times 9706 \times 76 \times 2}$$ (Chi square value for MTTF upper limit)

(where 9706 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 1.24 \times 10^{-9}$

$\lambda = 1.24$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the G4 Process results in a FIT Rate of 0.02 @ 25C and 0.37 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (ESD lot NZD0A3010C, D/C 1131, Latch-Up lot NZD0AA009C D/C 1108)

The WG25 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2000V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX2670GTB+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 150°C Biased Time = 1000 hrs.	DC Parameters & functionality	76	0	NZD0AQ001F, D/C 0613

Note 1: Life Test Data may represent plastic DIP qualification lots.