RELIABILITY REPORT

FOR

MAX2648EBT

CHIP SCALE DEVICES

January 30, 2004

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX2648 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX2648 high-linearity, silicon-germanium (SiGe) low-noise amplifier (LNA) is designed for 5GHz wireless LAN systems based on IEEE 802.11a and HiperLAN2 standards. The LNA provides high gain, low noise, and high linearity performance, allowing it to be used as a first-stage LNA, an LO buffer, or a transmitter driver amplifier. This highly versatile amplifier provides 17dB gain, 1.8dB noise figure, and 0dBm input third-order intercept point (IIP3) while consuming only 12mA.

The MAX2648 is designed on a low-noise, advanced SiGe process optimized for high-frequency applications. It operates over a +2.7V to +3.6V supply range. The device is packaged in a tiny 253 chipscale package (UCSP™) with six solder bumps, measuring 1.0mm x 1.5mm.

B. Absolute Maximum Ratings

Item	Rating
VCC to GND	-0.3V to +6.0V
RFOUT to GND	-0.3V to +6.0V
RFIN	-0.3V to +0.8V
RFIN Power (50. source)	+15dBm
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-55°C to +150°C
Continuous Power Dissipation (TA = +70°C)	
2 x 3 Bump UCSP	500mW
Derates above +70°C	
2 x 3 Bump UCSP	24mW/°C

II. Manufacturing Information

A. Description/Function:	5GHz to 6GHz Low-Noise Amplifier in 6-Pin UCSP
B. Process:	MB20 Bi-CMOS Process
C. Number of Device Transistors:	85
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines or USA
F. Date of Initial Production:	January, 2001

III. Packaging Information

A. Package Type:	**2 x 3 Bump UCSP**
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	N/A
E. Bondwire:	N/A
F. Mold Material:	N/A
G. Assembly Diagram:	# 05-7001-0462
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

IV. Die Information

A. Dimensions:	41.7 x 61.4 mils
B. Passivation:	Si_3N_4 (Silicon nitride)
C. Interconnect:	Au
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn) Metal 1, 2 & 3 5.6 microns (as drawn) Metal 4
F. Minimum Metal Spacing:	1.6 microns (as drawn) Metal 1, 2 & 3, 4.2 microns (as drawn) Metal 4
G. Bondpad Dimensions:	3.4 mil. Octagonal
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 9823 \times 100 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 4.85 \times 10^{-9}$ $\lambda = 4.85$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The WR88 die type has been found to have all pins able to withstand a transient pulse of ±500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit).

Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX2648EBT

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		74	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	UCSP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		N/A	N/A
Mechanical Stress (Note 2)					
Temperature Cycle	-40°C/125°C 1000 Cycles Slow Ramp (Note 3)	DC Parameters	UCSP	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Note 3: UCSP Temperature Cycle performed at with a ramp rate of 11°C/minute, dwell=15 minutes, one cycle/hour

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

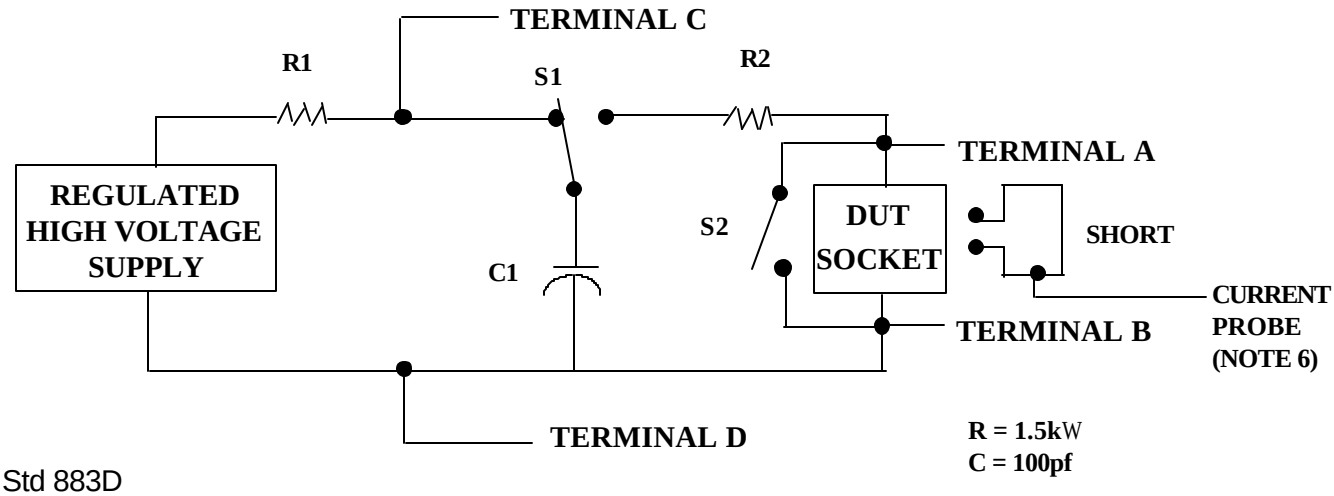
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

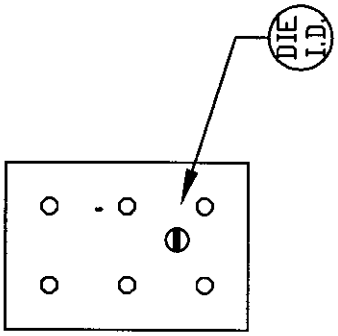
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

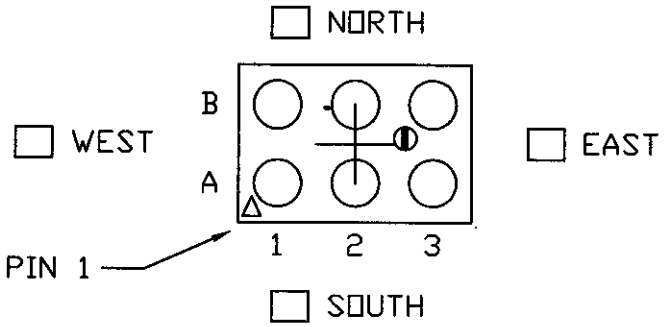


Mil Std 883D
Method 3015.7
Notice 8

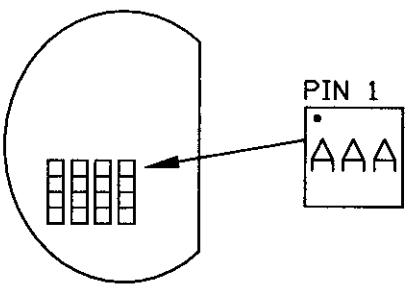
ORIGINAL CHIP



AFTER BUMP



SELECT THE BOX INDICATING THE WAFER FLAT SIDE WITH RESPECT TO PIN 1.



LASER MARK WAFER ORIENTATION
(Si BACKSIDE)

PKG. CODE: B6-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY
CAV./PAD SIZE: N/A	PKG. DESIGN			BOND DIAGRAM #: 05-7001-0462 REV: A