

RELIABILITY REPORT

FOR

MAX2392ETI+ (MAX2390-93, MAX2396, MAX2400)

PLASTIC ENCAPSULATED DEVICES

November 4, 2008

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR. SUNNYVALE, CA 94086

Approved by	
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Quality Assurance	
Director, Reliability Engineering	



Conclusion

The MAX2392ETI+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

- I.Device Description
- II.Manufacturing Information
- III.Packaging Information
-Attachments

VI.Reliability Evaluation

V.Quality Assurance Information

IV.Die Information

I. Device Description

A. General

The MAX2390-MAX2393/MAX2396/MAX2400 (referred to as the MAX2390 family) fully integrated direct-conversion receiver ICs are designed for W-CDMA and TDSCDMA applications. The MAX2390 family of receiver ICs have over 90dB of dynamic gain control, and typical noise figure of 2.7dB referred to LNA input. Each receiver consists of an ultra-low-current low-noise amplifier (LNA) with on-chip output matching and a two-step gain control. The zero-IF demodulator has a differential circuit topology for minimum LO leakage to receiver's input. The channel selectivity is done completely in the baseband section of the receiver with an on-chip lowpass filter. The AGC section has over 50dB of gain-control range. LO quadrature generation is done on-chip through a divide-by-2 prescaler. The DC offset cancellation in the I/Q baseband channels is done fully on-chip using a DC servo loop. To quickly correct for large DC offset transients in minimal time, very fast settling time is obtained by optimization of the DC-offset-cancellation circuit's time constant. The MAX2390 family includes a 3-wire serial bus for configuring the different receiver modes. They also include a SHDN-bar pin for full device shutdown. The receivers are fabricated using an advanced high-frequency SiGe BiCMOS process. The ICs operate from a single +2.7V to +3.3V supply and are housed in a small 28-pin leadless QFN-EP package (5mm x 5mm).



II. Manufacturing Information

D. Fabrication Location: E. Assembly Location:

F. Date of Initial Production:

Α.	Description/Function:	W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers
В.	Process:	SiGe HBT CMOS
C.	Number of Device Transistors:	

Oregon
ASAT China, UTL Thailand, Unisem Malaysia
January 25, 2003

III. Packaging Information

28-pin TQFN 5x5
Copper
100% matte Tin
Conductive Epoxy
Gold (1 mil dia.)
Epoxy with silica filler
#05-9000-1063
Class UL94-V0
Level 1
47°C/W
2.1°C/W
29°C/W
2.1°C/W

IV. Die Information

A.	Dimensions:	120 X 98 mils
В.	Passivation:	Si ₃ N ₄
C.	Interconnect:	Au
D.	Backside Metallization:	None
E.	Minimum Metal Width:	1.2 microns (as drawn) Metal 1, 2 & 3 5.6 microns (as drawn) Metal 4
F.	Minimum Metal Spacing:	1.6 microns (as drawn) Metal 1, 2 & 3, 4.2 microns (as drawn) Metal 4
G.	Bondpad Dimensions:	5 mil. Sq.
н.	Isolation Dielectric:	SiO ₂
I.	Die Separation Method:	Wafer Saw



V. Quality Assurance Information

A.	Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
В.	Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C.	Observed Outgoing Defect Rate:	< 50 ppm
D.	Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are pending. Using these results, the Failure Rate (λ) is calculated as follows:

 $\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 179 \times 2}$ (Chi square value for MTTF upper limit) (where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV) $\lambda = 6.0 \times 10^{-9}$ $\lambda = 6.0 \text{ F.I.T.}$ (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the G4 Process results in a FIT Rate of 0.2 @ 25C and 3.6 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The WC17 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2000 V per JEDEC JESD22-A114-D. Latch-Up testing has shown that this device withstands a current of 250 mA.



Table 1 Reliability Evaluation Test Results

MAX2392ETI+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	
Static Life Test (Note 1)					
	Ta = 135°C	DC Parameters	179	0	
	Biased	& functionality			
	Time = 192 hrs.				
Moisture Testing (Note 2)					
85/85	Ta = 85°C	DC Parameters	77	0	
	RH = 85%	& functionality			
	Biased				
	Time = 1000hrs.				
Mechanical Stress (Note 2)					
Temperature	-65°C/150°C	DC Parameters	77	0	
Cycle	1000 Cycles	& functionality			
	Method 1010				

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data