RELIABILITY REPORT

FOR

MAX2361EGM

PLASTIC ENCAPSULATED DEVICES

November 29, 2001

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX2361 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX236x family of quadrature transmitters includes quadrature modulator, variable gain IF and RF amplifiers, image rejecting up-converter mixer, and dual RF and IF synthesizers.

The MAX2361 is designed for dual band operation and supports CDMA for the PCS band as well as CDMA and AMPS for the cellular band. The desired mode of operation is selected by loading data on the SPI/Microwire compatible 3-wire serial bus. The MAX2361 then routes the signals to the appropriate ports depending on which band is selected. No off-chip band switching hardware is required since the MAX2361 includes two IF VCOs, two IF input and output ports, two RF LO input ports, and three PA driver ports.

B. Absolute Maximum Ratings

Item	Rating
V_{CC} to GND	-0.3V to +6.0V
RFL,RFH0,RFH1,VCCIFCP,VCCRFCP,VCCDRV to Gnd	-0.3V to 5.5V
DI,CLK,CS,GC,SHDN,TXGATE,IDLE,LOCK to Gnd	-0.3V to (VCC + 0.3V
AC Input Pins (IFINL_,IFINH_,Q_,I_,TANKL_,TANKH_, REF,RFPLL,LOL,LOH)	1.0V peak
Digital Input Current (SHDN,TXGATE,IDLE,CLK,DI,CS)	+/-10mA
Junction Temperature	+150°C
Storage Temp.	-65°C to +150°C
Lead Temp. (soldering 10 sec.)	+300°C
Power Dissipation	
48-Pin QFN-EP	2.1W
Derates above +70°C	
48-Pin QFN-EP	27mW/°C

II. Manufacturing Information

A. Description/Function:	Complete Dual-Band Transmitters
B. Process:	MB10 Bi-CMOS Process
C. Number of Device Transistors:	11,083
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Korea
F. Date of Initial Production:	April, 2001

III. Packaging Information

A. Package Type:	48-Pin QFN
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Hi-Bond Conductive Epoxy
E. Bondwire:	Gold (1.2 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-2201-0039
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 3

IV. Die Information

A. Dimensions:	134 x 32 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Au
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn) Metal 1&2, 2.8 microns (as drawn) Metal 3
F. Minimum Metal Spacing:	1.6 microns (as drawn) Metal 1&2, 2.8 microns (as drawn) Metal 3
G. Bondpad Dimensions:	3 mil. Octagonal
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{1000 \times 9823 \times 50 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 10.78 \times 10^{-9}$ $\lambda = 10.78$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic #06-5838 shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1L**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The WR53-1 die type has been found to have all pins able to withstand a transient pulse of ±200V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit).

. Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX2361EUB

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 150°C Biased Time = 1000 hrs.	DC Parameters & functionality	50	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the Micro Max package.
Note 2: Generic package/process data.

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

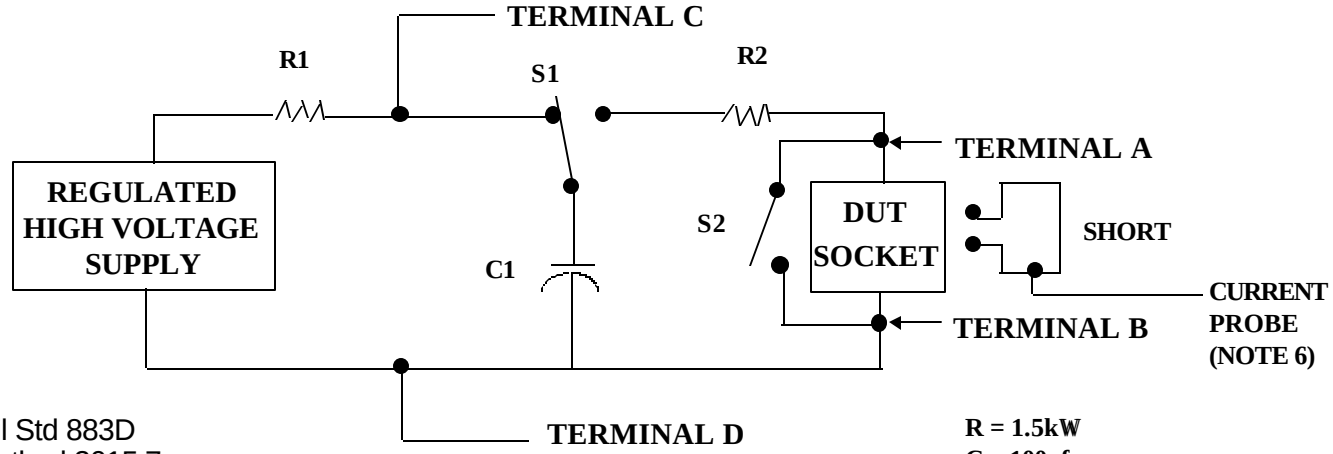
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

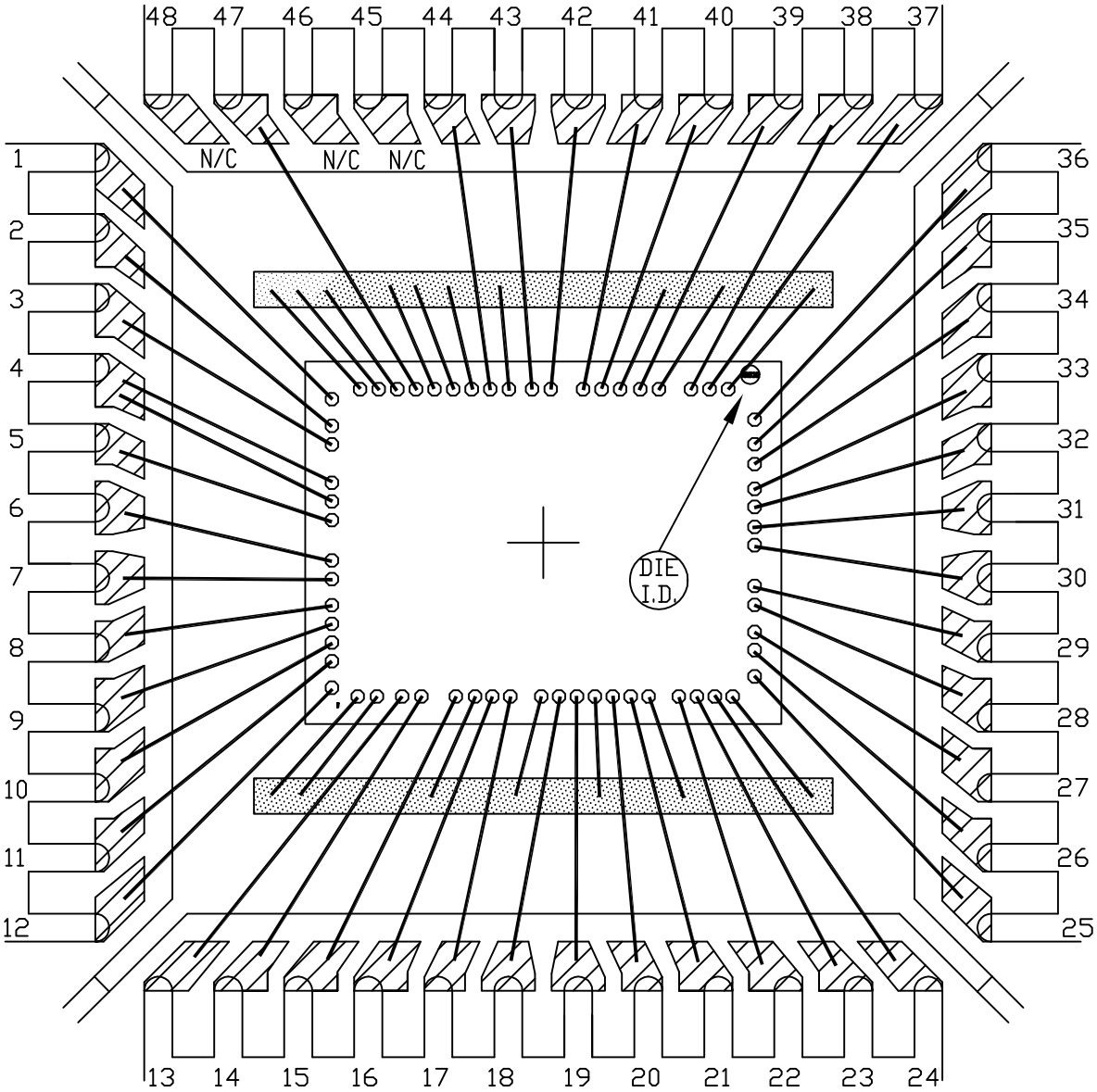
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

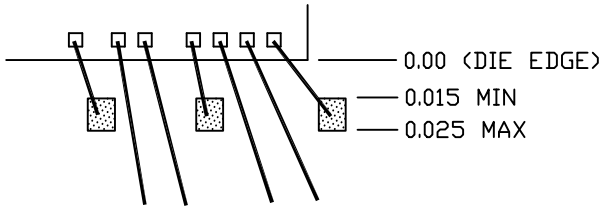


Mil Std 883D
Method 3015.7
Notice 8

EXPOSED PAD PKG.



DOWNBOND DETAILS:
DOWNBOND LENGTHS ARE CRITICAL.
CONTROL DOWNBOND LOCATIONS AS SHOWN.



BONDABLE AREA

PKG. BODY SIZE: 7x7 mm

PKG. CODE: G4877-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY
CAV./PAD SIZE: 209x209	PKG.			BOND DIAGRAM #: 05-2201-0039 REV: D
	DESIGN		7/24/01	