RELIABILITY REPORT

FOR

MAX2354EGI

PLASTIC ENCAPSULATED DEVICES

August 14, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Reviewed by

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Conclusion

The MAX2354 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX2354 multiband LNA/Mixer IC is optimized for CDMA, GSM, and TDMA applications in the cellular band. The MAX2354 IC features a cellular band LNA Mixer with LO buffer. The cellular signal can be routed to either IF port. For example, one IF port can be connected to an IF filter with 30kHz band-width, while the other port can drive an IF filter with a wider bandwidth.

To optimize dynamic range at minimum current, the MAX2354 implements multiple LNA and mixer states, including high gain/high linearity, high gain/low linearity, mid gain, low gain, and ultra low gain. In high-gain/high-linearity mode, the high-intercept LNA minimizes desensitization in the presence of a large interfering signal. For the other gain states, the LNA current is reduced to improve standby time. Each band is implemented with a separate mixer to optimize performance for the specific band, and each mixer provides multiple linearity modes to optimize linearity and current consumption. The ultra-low gain mode operates with very little current, which results in significant power savings because the handset typically spends most of its time in this mode.

B. Absolute Maximum Ratings

Item	Rating
V_{CC} to GND	-0.3V to +4.3V
Digital Input Voltage to Gnd	-0.3V to (VCC + 0.3V)
LNA Inout (Low-Gain Mode) Level	15dBm
LO Input Level	5dBM
Digital Input Current	10mA
Junction Temperature	+150°C
Operating Temperature Range	-40°C to +85°C
Storage Temp.	-65°C to +150°C
Lead Temp. (soldering 10 sec.)	+300°C
Continuous Power Dissipation (TA = +70°C)	
28-Pin QFN	1.6W
Derates above +70°C	
28-Pin QFN	21mW/°C

II. Manufacturing Information

A. Description/Function:	Quadruple-Mode PCS/Cellular/GPS LNA/Mixer
B. Process:	MB20 Bi-CMOS Process
C. Number of Device Transistors:	2538
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Korea
F. Date of Initial Production:	August, 2002

III. Packaging Information

A. Package Type:	**28-Pin QFN**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-Filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-9000-0246
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

IV. Die Information

A. Dimensions:	89 x 87 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Au
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn) Metal 1, 2 & 3 5.6 microns (as drawn) Metal 4
F. Minimum Metal Spacing:	1.6 microns (as drawn) Metal 1, 2 & 3, 4.2 microns (as drawn) Metal 4
G. Bondpad Dimensions:	3.4 mil. Octagonal
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 9823 \times 90 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 5.39 \times 10^{-9}$ $\lambda = 5.39$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic #06-7030 shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The WC19 die type has been found to have all pins able to withstand a transient pulse of ±600V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit).

Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX2354EGI

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality	90	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic DIP qualification packages.
Note 2: Generic package/process data.

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

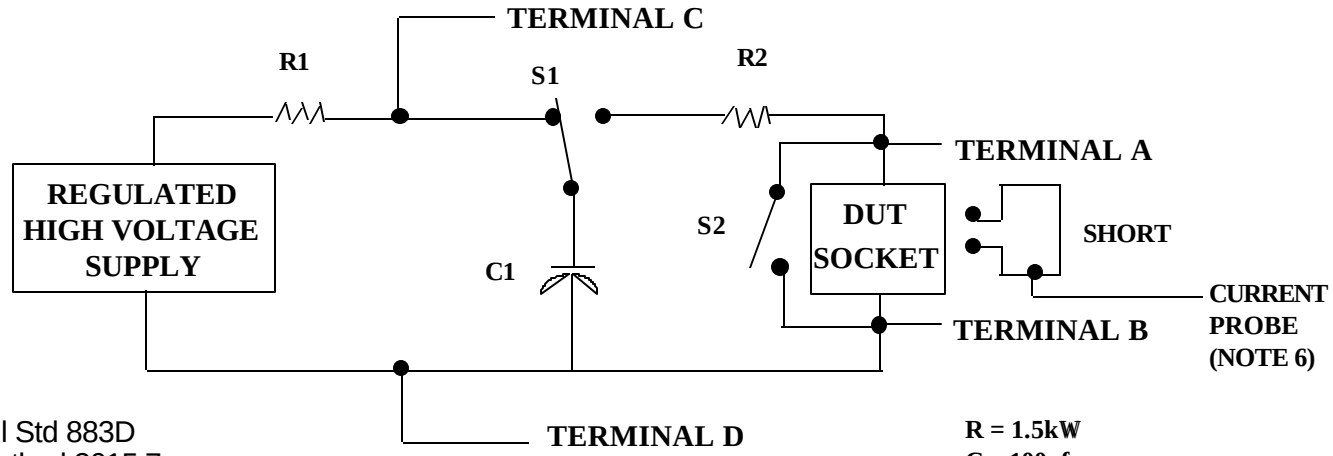
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

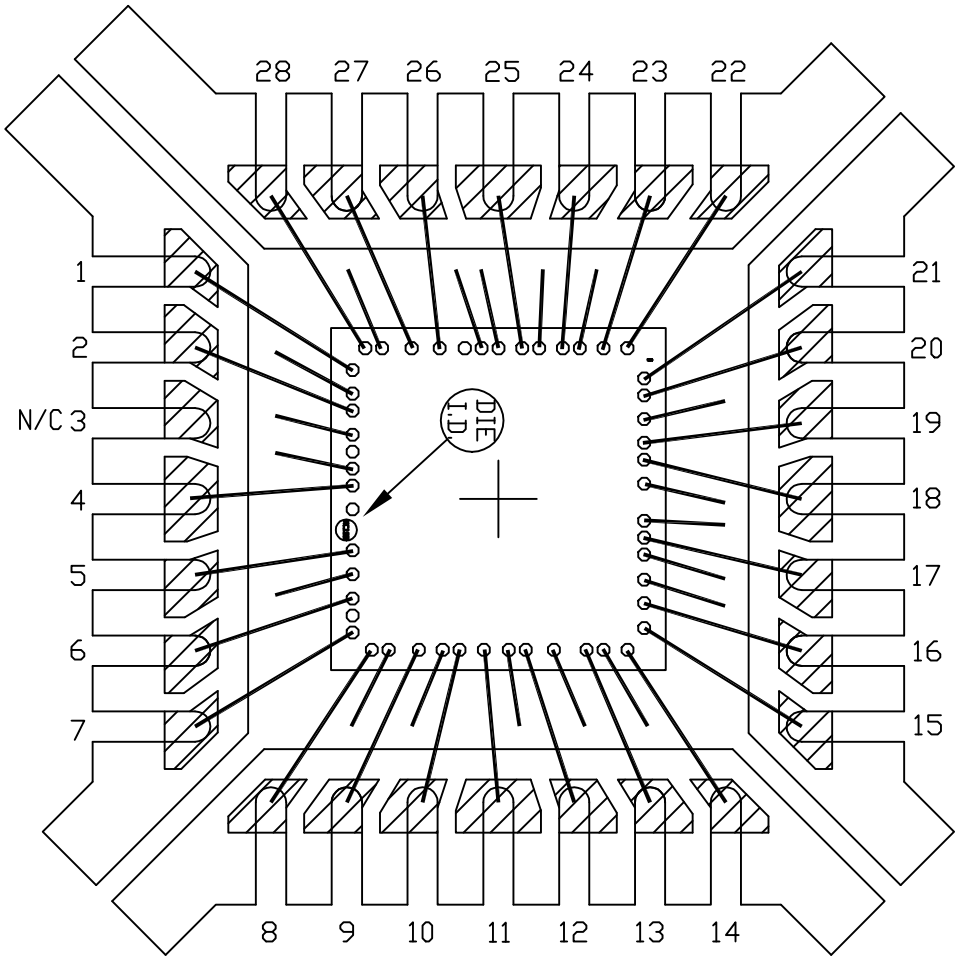
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

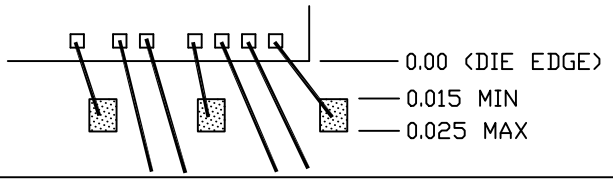


Mil Std 883D
Method 3015.7
Notice 8

EXPOSED PAD PKG.



DOWNBOND DETAILS:
DOWNBOND LENGTHS ARE CRITICAL.
CONTROL DOWNBOND LOCATIONS AS SHOWN.



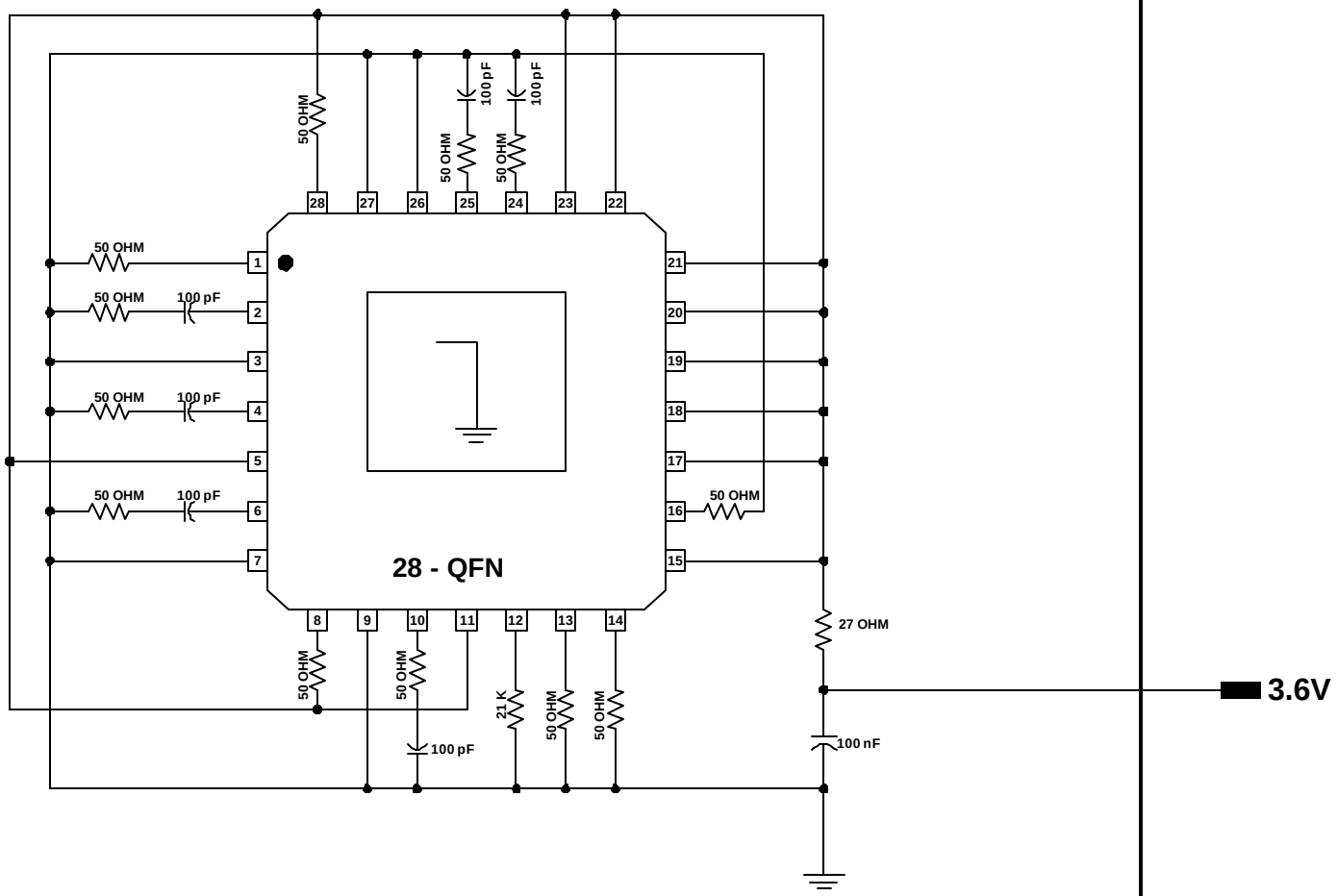
BONDABLE AREA

PKG. BODY SIZE: 5x5 mm

PKG. CODE: G2855-2		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 130x130	PKG.			BOND DIAGRAM #: 05-9000-0246	REV: A
	DESIGN				

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 2538

MAX. EXPECTED CURRENT = 40mA

DRAWN BY: HAK TAN

NOTES: