MAX232ExxE Rev. A

RELIABILITY REPORT

FOR

MAX232ExxE

PLASTIC ENCAPSULATED DEVICES

May 11th, 2003

MAXIM INTEGRATED PRODUCTS

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Written by

e/h

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Conclusion

The MAX232E successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX232E line drivers/receiver is designed for RS-232 and V.28 communications in harsh environments. Each transmitter output and receiver input is protected against ±15kV electrostatic discharge (ESD) shocks, without latchup. The various combinations of features are outlined in the *Selection Guide*. The driver and receiver for the device meets all EIA/TIA-232E and CCITT V.28 specifications at data rates up to 120kbps, when loaded in accordance with the EIA/TIA-232E specification.

The MAX232E comes in a 16-pin narrow SO, wide SO, and DIP packages. The MAX232E operates with four 1μ F capacitors, further reducing cost and board space.

B. Absolute Maximum Ratings

ltem	Rating		
VCC	-0.3V to +6V		
V+	(VCC - 0.3V) to +14V		
V-	-14V to +0.3V		
Input Voltages			
T_IN	-0.3V to (V+ + 0.3V)		
R_IN	±30V		
Output Voltages			
T_OUT	(V 0.3V) to (V+ + 0.3V)		
R_OUT	-0.3V to (VCC + 0.3V)		
Short-Circuit Duration, T_OUT	Continuous		
Operating Temperature Ranges			
MAX232EC	0°C to +70°C		
MAX2_32EE	-40°C to +85°C		
Storage Temperature Range	-65°C to +165°C		
Lead Temperature (soldering, 10sec)	+300°C		
Continuous Power Dissipation (TA = +70°C)			
16-Pin NSO	696mW		
16-Pin WSO	762mW		
16-Pin PDIP	842mW		
Derates above +70°C			
16-Pin NSO	8.7mW/°C		
14-Pin WSO	9.52mW/°C		
16-Pin PDIP	10.53mW/°C		

II. Manufacturing Information

A. Description/Function:	±15kV ESD-Protected, +5V RS-232 Transceivers
B. Process:	SMG (M5) - 5 micron metal gate CMOS
C. Number of Device Transistors:	123
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines, Thailand or Malaysia
F. Date of Initial Production:	June, 1994

III. Packaging Information

A. Package Type:	16-Lead SO	16-Lead WSO	16-Lead PDIP
B. Lead Frame:	Copper	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silve-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	Epoxy witj silica filler
G. Assembly Diagram:	# 05-1901-0064	# 05-1901-0065	#05-1901-0063
H. Flammability Rating:	Class UL94-V0	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD-020-A:	Level 1	Level 1	Level 1

IV. Die Information

A. Dimensions:	80 x 117 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	5 microns (as drawn)
F. Minimum Metal Spacing:	5 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager, Rel Operations) Bryan Preeshl (Executive Director of QA) Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \underbrace{1}_{\text{MTTF}} = \underbrace{1.83}_{192 \text{ x } 4389 \text{ x } 240 \text{ x } 2} \text{ (Chi square value for MTTF upper limit)}$$

$$L$$

$$Temperature Acceleration factor assuming an activation energy of 0.8eV$$

$$\lambda = 4.52 \text{ x } 10^{-9}$$

$$\lambda = 4.52 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-0259) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The RS22 die type has been found to have all pins able to withstand a transient pulse of $\pm 2500V$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Additionally, the MAX232E has achieved $\pm 15kV$ ESD protection using both methods 3015 and IEC 801-2 (air-gap discharge) on the I/O pins. Latch-Up testing has shown that this device withstands a current of ± 100 mA.

Table 1 Reliability Evaluation Test Results

MAX232ExxE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test	t (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		240	0
Moisture Testi	ng (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	PDIP NSO WSO	77 77 77	0 0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Str	ress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots. Note 2: Generic Package/Process data

Attachment #1

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V _{PS1} <u>3/</u>	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

TABLE II. Pin combination to be tested. 1/2/

- 1/ Table II is restated in narrative form in 3.4 below.
- No connects are not to be tested. $\underline{3}$ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_{S}$, $-V_{S}$, V_{REF} , etc).

- 3.4 Pin combinations to be tested.
 - Each pin individually connected to terminal A with respect to the device ground pin(s) connected a. to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
 - Each pin individually connected to terminal A with respect to each different set of a combination b. of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
 - Each input and each output individually connected to terminal A with respect to a combination of c. all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.







PKG.CDDE: W16-1 APPROVALS DATE	BUILDSHEET NUMBER: REV.

