RELIABILITY REPORT

FOR

MAX2309EGI

PLASTIC ENCAPSULATED DEVICES

August 3, 2001

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX2309 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX2309 is an IF receiver designed for dual-band, dual-mode, and single-mode N-CDMA and W-CDMA cellular phone systems. The signal path consists of a variable-gain amplifier (VGA) and I/Q demodulator. The devices feature guaranteed +2.7V operation, a gain control range of over 110dB, and high input IP3 (-33dBm at 35dB gain, 1.7dBm at -35dB gain).

Unlike similar devices, the MAX2309 includes dual oscillators and synthesizers to form a self-contained IF subsystem. The synthesizer's reference and RF dividers are fully programmable through a 3-wire serial bus, enabling dual-band system architectures using any common reference and IF frequency. The differential baseband outputs have enough bandwidth to suit both N-CDMA and W-CDMA systems, and offer saturated output levels of 2.7Vp-p at a low +2.75V supply voltage. Including the low-noise voltage-controlled oscillator (VCO) and synthesizer, the MAX2309 draws only 26mA from a +2.75V supply in CDMA (differential IF) mode.

The MAX2309 are available in 28-pin QFN packages.

B. Absolute Maximum Ratings

Item	Rating
VCC to GND	-0.3V to +6V
SHDN to GND	-0.3V to (VCC +0.3V)
STBY, BUFEN, MODE, EN, DATA, CLK, DIVSEL	-0.3V to (VCC + 0.3V)
AC Signals TANKH±, TANKL±, REF, FM±, CDMA±	1.0V peak
Junction Temperature	+150°C
Storage Temp.	-65°C to +160°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	
28-Pin QFN	2W
Derates above +70°C	
28-Pin QFN	28.5 mW/°C

II. Manufacturing Information

A. Description/Function: CDMA IF VGA and I/Q Demodulator with VCO and Synthesizer

B. Process: GST20

C. Number of Device Transistors: 6442

D. Fabrication Location: Oregon, USA

E. Assembly Location: Korea

F. Date of Initial Production: April, 2001

III. Packaging Information

A. Package Type:	**28-Lead QFN**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	HB2600 Conductive Epoxy
E. Bondwire:	Gold (1.2 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-7001-0492
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

IV. Die Information

A. Dimensions: 57 x 103 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Poly/Au

D. Backside Metallization: None

E. Minimum Metal Width: 1.4 microns (as drawn)

F. Minimum Metal Spacing: 1.4 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord	(Reliability Lab Manager)
Bryan Preeshl	(Executive Director of QA)
Kenneth Huening	(Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 45 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV (applies to 4389)

$\lambda = 24.1 \times 10^{-9}$ λ = 24.1 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1L**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The WR29 die type has been found to have all pins able to withstand a transient pulse of ±500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA and/or ±20V.

Table 1

Reliability Evaluation Test Results

MAX2309EGI

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	45	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the Small Outline package.
Note 2: Generic Process/Package data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.