MAX2205EBS
Rev. A

RELIABILITY REPORT

FOR

MAX2205EBS

Chip Scale Devices

April 8, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX2205 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. ....Device Description
II. ....Manufacturing Information
III. ....Packaging Information
V. ....Quality Assurance Information
VI. ....Reliability Evaluation
IV. ....Die Information
.....Attachments

I. Device Description

A. General

The MAX2205 wideband (800MHz to 2GHz) power detector is ideal for CDMA applications. The MAX2205 takes an RF signal from a directional coupler at the input, and output a highly repeatable voltage. The output voltage increases monotonically with increasing input power. The output is compensated for temperature and process shifts, reducing the worst-case variation to less than ±1dB at full power and ±2.5dB at the lowest power.

The MAX2205 has an integrated filter to allow for average power detection of CDMA signals over a 25dB dynamic range. The MAX2205 has a high-impedance input to provide a low-loss resistive tap in CDMA applications. The device allows the user to control the averaging time constant externally.

The MAX2205 comes in a space-saving 2 x 2, 0.5mm-pitch UCSP™ and requires only three external components.

B. Absolute Maximum Ratings

Item	Rating
VCC to GND	-0.3V to +6.5V
RFIN/SHDN to GND	-0.3V to (VCC + 0.3V)
RF Input Voltage (800MHz)	1.5VP
RF Input Voltage (2GHz) (MAX2205)	0.8VP
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +160°C
Bump Temperature (soldering) (Note 1)	
Infrared (15s)	+220°C
Vapor Phase (60s)	+215°C
Continuous Power Dissipation (TA = +70°C)	
2 x 2 UCSP	303mW
Derates above +70°C	
2 x 2 UCSP	3.8mW/°C

II. Manufacturing Information

A. Description/Function: RF Power Detectors in UCSP

B. Process: GST2 – High Speed Double Poly-Silicon Bipolar Process

C. Number of Device Transistors: 344

D. Fabrication Location: Oregon, USA

E. Assembly Location: Korea

F. Date of Initial Production: April, 2002

III. Packaging Information

A. Package Type: **2 x 2 UCSP**

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: N/A

E. Bondwire: N/A

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: # 05-3201-0008

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112: Level 1

IV. Die Information

A. Dimensions: 40 x 40 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Poly / Au

D. Backside Metallization: None

E. Minimum Metal Width: 2 microns (as drawn)

F. Minimum Metal Spacing: 2 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

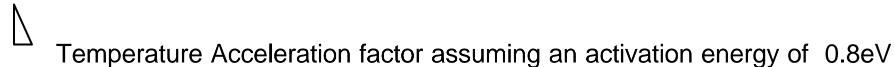
D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 9823 \times 45 \times 2}$$ (Chi square value for MTTF upper limit)



Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 10.78 \times 10^{-9}$

$\lambda = 10.78$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. #06-5818) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-B2A**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The WC15-4 die type has been found to have all pins able to withstand a transient pulse of ±2500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX2205EBS

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality		45	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	CSP	80	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		N/A	N/A
Mechanical Stress (Note 2)					
Temperature Cycle	-40°C/125°C 1000 Cycles Slow Ramp	DC Parameters & functionality		77	0

Note 1: Life Test Data represents packaged qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

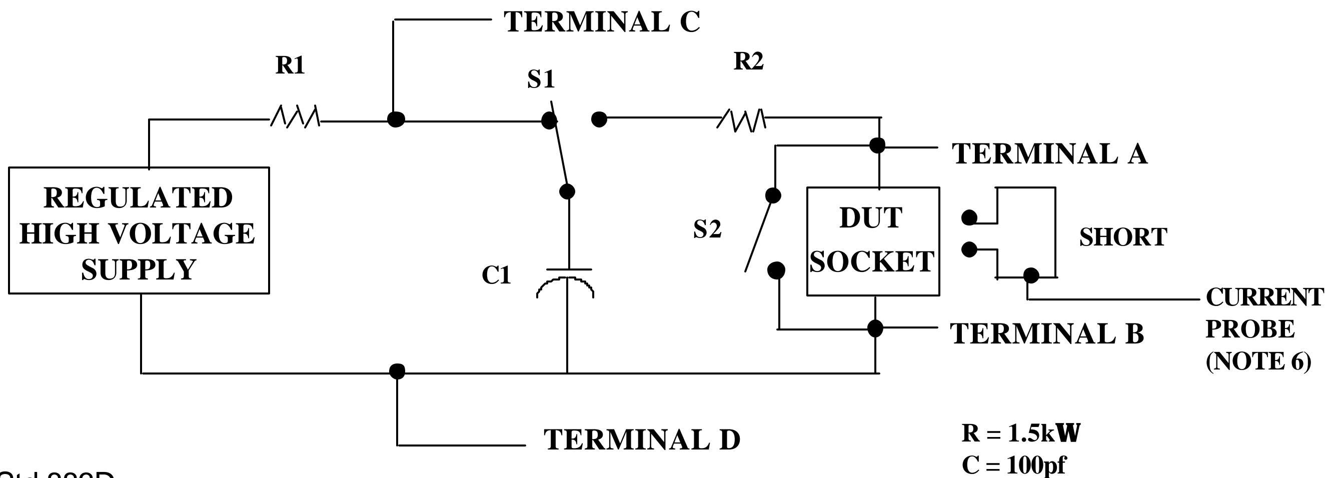
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, +V_S, -V_S, V_{REF}, etc).

3.4 Pin combinations to be tested.

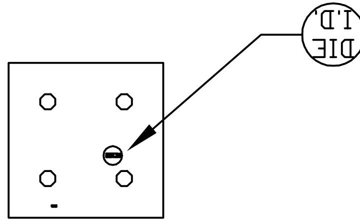
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

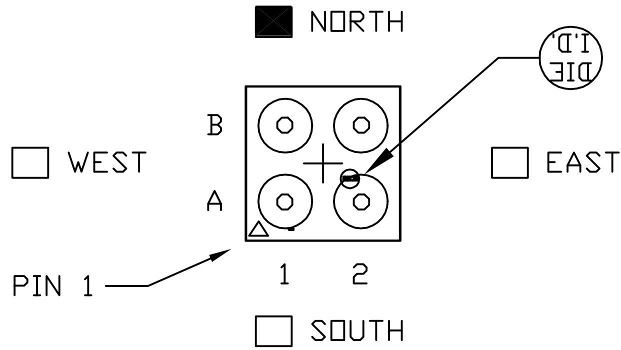
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



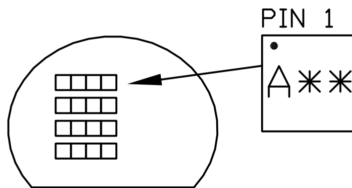
ORIGINAL CHIP



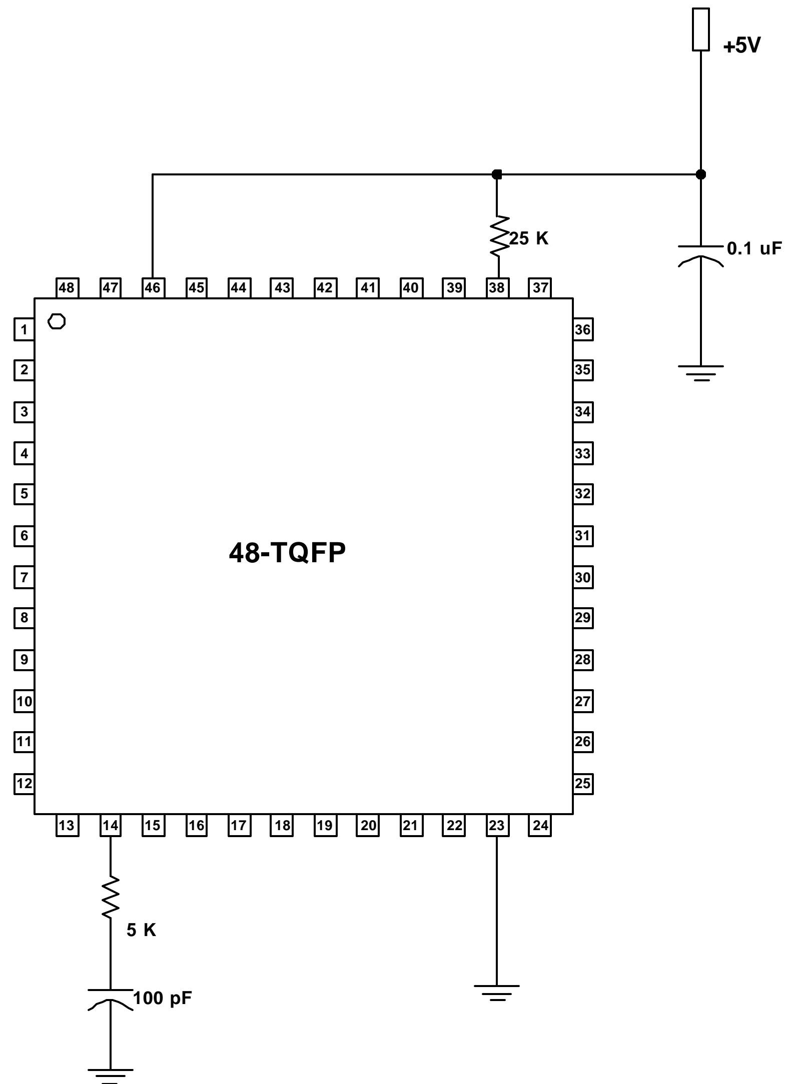
AFTER BUMP



SELECT THE BOX INDICATING THE WAFER FLAT SIDE
WITH RESPECT TO PIN 1.



PART MARKING ORIENTATION
IN REFERENCE TO WAFER FLAT
(MARK IS ON WAFER BACKSIDE)



DEVICES: MAX 2206/7/8

MAX. EXPECTED CURRENT = 5mA

DRAWN BY : HAK TAN

NOTES: