MAX2150ETI
Rev. A

RELIABILITY REPORT

FOR

MAX2150ETI

PLASTIC ENCAPSULATED DEVICES

January 7, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX2150 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX2150 is a complete wideband direct upconversion quadrature modulator IC incorporating a 28-bit sigma-delta fractional-N synthesizer. The device is targeted for applications in the 700MHz to 2300MHz frequency range.

The super-high-resolution sigma-delta fractional-N synthesizer is capable of better than 50mHz resolution when used with a 10MHz reference. Other features include fully differential I/Q modulation inputs, an internal LO buffer, and a 50Ω wideband output driver amplifier.

A standard 3-wire interface is provided for synthesizer programming and overall device configuration. An on-chip low-noise crystal oscillator amplifier is also included and can be configured as a buffer when an external reference oscillator is used.

The device typically achieves 34dBc of carrier and sideband suppression at a -1dBm output level. The wideband, internally matched RF output can also be disabled while the synthesizer and 3-wire bus remain powered up for continuous programming.

The device consumes 72mA from a single +3.0V supply and is packaged in an ultra-compact 28-pin thin QFN package (5mm x 5mm) with an exposed pad.

B. Absolute Maximum Ratings

Item	Rating
VCC to GND	-0.3V to +6.0V
RF Signals: LO+, LO-, OSCIN	+10dBm
I+ to I-, Q+ to Q-	2V
LO+, LO-, I+, I-, Q+, Q-, BUFEN, TXEN, CLK, DATA, EN , SYNEN, OSCIN, OSCOUT, BUFOUT, CHP, SHDN,LOCK, VCC_CP to GND	-0.3V to (VCC + 0.3V)
Digital Input Current	±10mA
Short-Circuit Duration RFOUT, BUFOUT, OSCOUT, Lock, CHP	10s
Operating Temperature Range	-40°C to +85°C
Junction Temperature Range	+150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (soldering 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
28-Pin QFN	2W
Derates above +70°C	
28-Pin QFN	28.5mW/°C

II. Manufacturing Information

A. Description/Function: Wideband I/Q Modulator with Sigma-Delta Fractional-N Synthesizer

B. Process: MB10 Bi-CMOS Process

C. Number of Device Transistors: 16,321

D. Fabrication Location: Oregon, USA

E. Assembly Location: Thailand

F. Date of Initial Production: April, 2002

III. Packaging Information

A. Package Type: 28-Pin QFN

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: Silver-filled Epoxy

E. Bondwire: Gold (1.0 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: # 05-4401-0001

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1

IV. Die Information

A. Dimensions: 100 x 100 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Au

D. Backside Metallization: None

E. Minimum Metal Width: 1.2 microns (as drawn) Metal 1&2, 2.8 microns (as drawn) Metal 3

F. Minimum Metal Spacing: 1.6 microns (as drawn) Metal 1&2, 2.8 microns (as drawn) Metal 3

G. Bondpad Dimensions: 3 mil. Octagonal

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{1000 \times 9823 \times 45 \times 2}$$ (Chi square value for MTTF upper limit)

(9823 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 10.78 \times 10^{-9}$ λ = 10.78 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic #06-7038 shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-B2A**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The WG05 die type has been found to have all pins able to withstand a transient pulse of <200V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit).

Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX2150ETI

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 150°C Biased Time = 1000 hrs.	DC Parameters & functionality	45	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic package/process data.

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

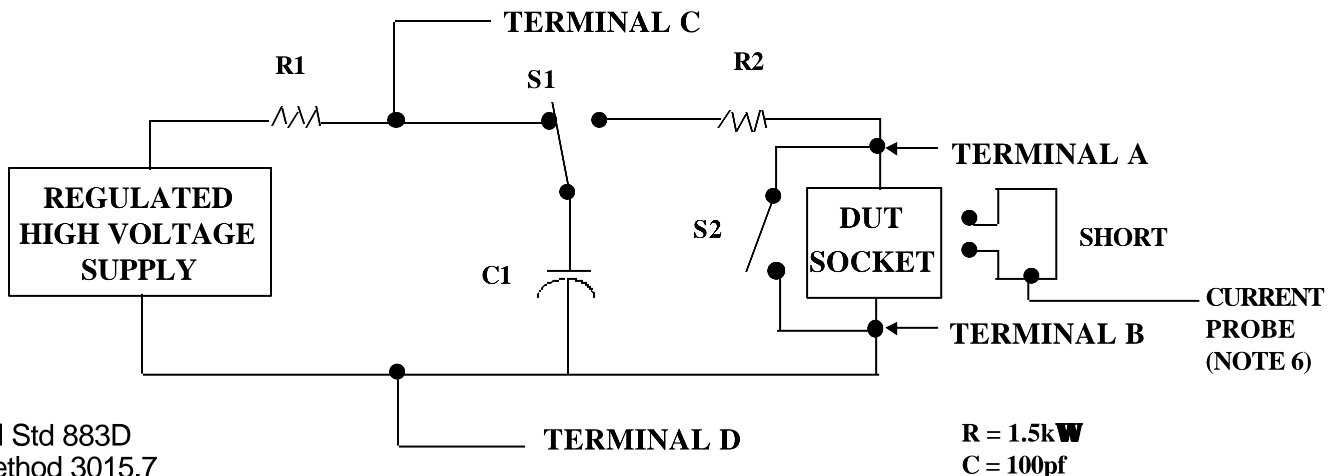
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

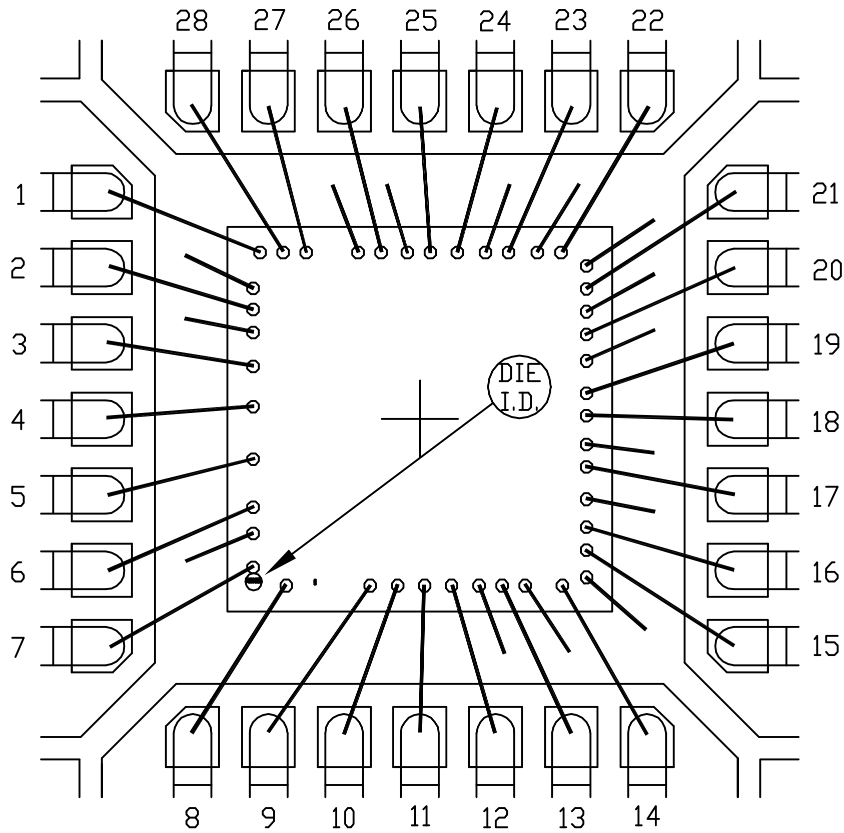
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

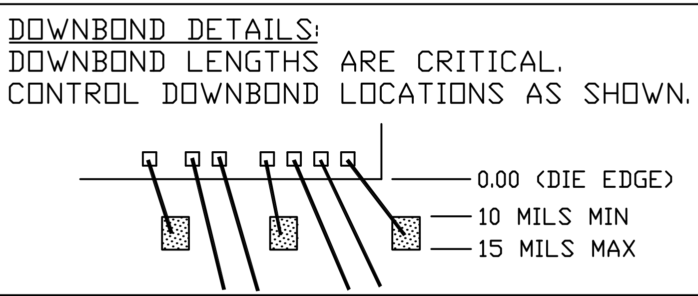
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



5x5x0.8 MM QFN THIN PKG.

EXPOSED PAD PKG.

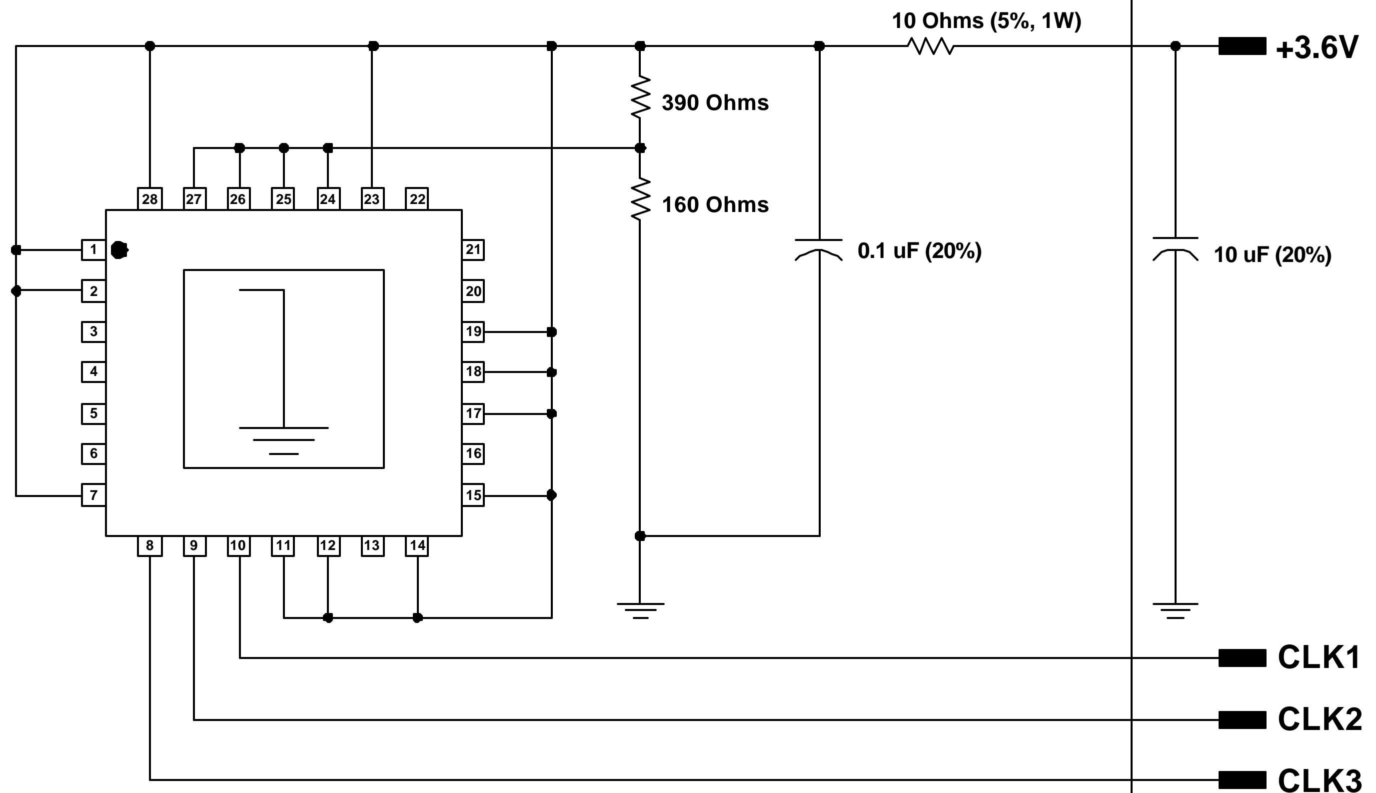




PKG. CODE: T2855-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 138x138	PKG.			BOND DIAGRAM #: 05-4401-0001	REV: C
	DESIGN				

ONCE PER SOCKET

ONCE PER BOARD



PROGRAMMING SEQUENCE:

- START WITH CLK1 = 1, CLK2 = 1, CLK3 = 0
- MOVE CLK1 = 0
- MOVE CLK3 TO "1" AND THEN BACK TO "0" SIXTEEN TIMES
- MOVE CLK1 = 1

DEVICES: MAX 2150
PACKAGE: 28-QFN (5x5)
MAX. EXPECTED CURRENT = 100 mA

DRAWN BY: HAK/TEK TAN
NOTES: