

RELIABILITY REPORT
FOR
MAX2140ETH+
PLASTIC ENCAPSULATED DEVICES

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MAXIM INTEGRATED

160 RIO ROBLES
SAN JOSE, CA 95134

Approved by
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Conclusion

The MAX2140ETH+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX2140 complete receiver is designed for satellite digital audio radio services (SDARS). The device includes a fully monolithic VCO and only needs a SAW at the IF and a crystal to generate the reference frequency. To form a complete SDARS radio, the MAX2140 requires only a low-noise amplifier (LNA), which can be controlled by a baseband controller. The small number of external components needed makes the MAX2140-based platform the lowest cost and the smallest solution for SDARS. The receiver includes a self-contained RF AGC loop and baseband-controlled IF AGC loop, effectively providing a total dynamic range of over 92dB. Channel selectivity is ensured by the SAW filter and by on-chip monolithic lowpass filters. The fractional-N PLL allows a very small frequency step, making possible the implementation of an AFC loop. Additionally, the reference is provided by an external XTAL and on-chip oscillator. A reference buffer output is also provided. A 2-wire interface (I²C bus compatible) programs the circuit for a wide variety of conditions, providing features such as: - Programmable gains - Lowpass filters tuning - Individual functional block shutdown The MAX2140 minimizes the requirement on the baseband controller. No compensation or calibration procedures are required. The device is available in a 7mm x 7mm 44-pin thin QFN package.

II. Manufacturing Information

A. Description/Function:	Complete SDARS Receiver
B. Process:	G4
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon
E. Assembly Location:	Taiwan, Thailand
F. Date of Initial Production:	December 17, 2003

III. Packaging Information

A. Package Type:	44-pin TQFN 7x7
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-0486
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	37°C/W
K. Single Layer Theta Jc:	1.3°C/W
L. Multi Layer Theta Ja:	27°C/W
M. Multi Layer Theta Jc:	1.3°C/W

IV. Die Information

A. Dimensions:	128X115 mils
B. Passivation:	Si ₃ N ₄
C. Interconnect:	Au
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.6 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{1000 \times 9706 \times 281 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 9706 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 0.34 \times 10^{-9}$$

$$\lambda = 0.34 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the G4 Process results in a FIT Rate of 0.04 @ 25C and 0.66 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (lot NEZ0E2864E, D/C 1153)

The WG18 die type has been found to have all pins able to withstand a HBM transient pulse of +/-500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX2140ETH+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 150°C	DC Parameters XXXXXXXXXX & functionality	78	0	NEZ0EA592A, D/C 0739
	Biased		47	0	NEZ0EA586C, D/C 0743
	Time = 1000 hrs.			0	NEZ0EA456A, D/C 0633

Note 1: Life Test Data may represent plastic DIP qualification lots.