RELIABILITY REPORT

FOR

MAX2116UGL

PLASTIC ENCAPSULATED DEVICES

November 3, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX2116 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX2116 low-cost direct-conversion tuner IC is designed for use in digital direct broadcast satellite (DBS) television applications, professional VSAT systems, and two-way Internet through satellite applications. This device sets the standard for integration and performance, significantly reducing the required RF know-how for design implementation. Uniquely architected, the MAX2116 simplify direct main board and tuner module designs.

The MAX2116 device directly converts L-band signals to baseband using a broadband I/Q downconverter. The operating frequency range extends from 925MHz to 2175MHz.

The IC includes an LNA with gain control, I and Q downconverting mixers, and baseband lowpass filters gain and cutoff frequency control. Together, the RF and baseband variable gain amplifiers provide more than 79dB of gain control range.

The device includes a fully monolithic VCO, as well as a complete frequency synthesizer. Additionally, an on-chip crystal oscillator is provided along with a buffered output for driving additional tuners and demodulators. Synthesizer programming and device configuration are accomplished with a 2-wire serial interface. For multi-tuner applications, the device can be configured to have one of eight possible 2-wire interface addresses.

Simplifying the interface to low-voltage CMOS demodulators, the MAX2116 incorporates two 2.85V regulated outputs for pulling up open-drain interface connections, thus preventing noisy 3V rails from corrupting the sensitive analog signal of the tuners.

The MAX2116 device is the most versatile family of DBS products available. With both single-ended and differential baseband outputs, this device is compatible with virtually all QPSK/8-PSK demodulators. The tuner is available in a very small 40-pin QFN package.

B. Absolute Maximum Ratings

Item	Rating
VCC to GND	-0.3V to +5.5V
All Other Pins to GND	-0.3V to (VCC + 0.3V)
RFIN+ to RFIN-, XTL+ to XTL-, IDC+ to IDC-,QDC+ to QDC-	±2.0V
CNTOUT, XTALOUT, CPOUT, VREG1/2, I/QOUT± to GND Short-Circuit Duration	10s
Continuous Current (any pin other than VCC or GND)	10mA
Operating Temperature Range	0°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +160°C
Soldering Temperature (10s)	+300°C
Continuous Power Dissipation (TA = +85°C)	
40-Pin QFN-EP	1.86W
Derates above +70°C	
40-Pin QFN-EP	23.3mW/°C

II. Manufacturing Information

A. Description/Function:	Complete DBS Direct-Conversion Tuner IC with Monolithic VCOs
B. Process:	MB14 Bi-CMOS Process
C. Number of Device Transistors:	10,935
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Korea
F. Date of Initial Production:	April, 2002

III. Packaging Information

A. Package Type:	**40-Pin QFN(6x6)**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Hi-Bond Conductive Epoxy
E. Bondwire:	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-7001-0588
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

IV. Die Information

A. Dimensions:	125 x 111 mils
B. Passivation:	Si_3N_4 (Silicon nitride)
C. Interconnect:	Au
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn) Metal 1&2, 2.8 microns (as drawn) Metal 3
F. Minimum Metal Spacing:	1.6 microns (as drawn) Metal 1&2, 2.8 microns (as drawn) Metal 3
G. Bondpad Dimensions:	3 mil. Octagonal
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 9823 \times 44 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 11.03 \times 10^{-9}$ $\lambda = 11.03$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic #06-7048 shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The WG14-1 die type has been found to have all pins able to withstand a transient pulse of ±600V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit).

. Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX2116UGL

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality	44	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic package/process data.

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

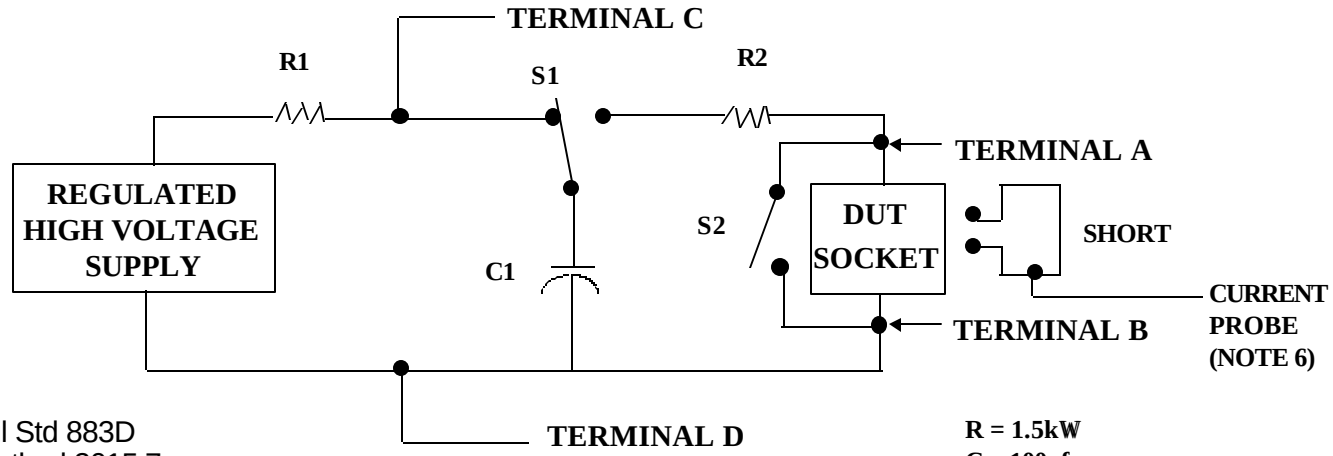
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

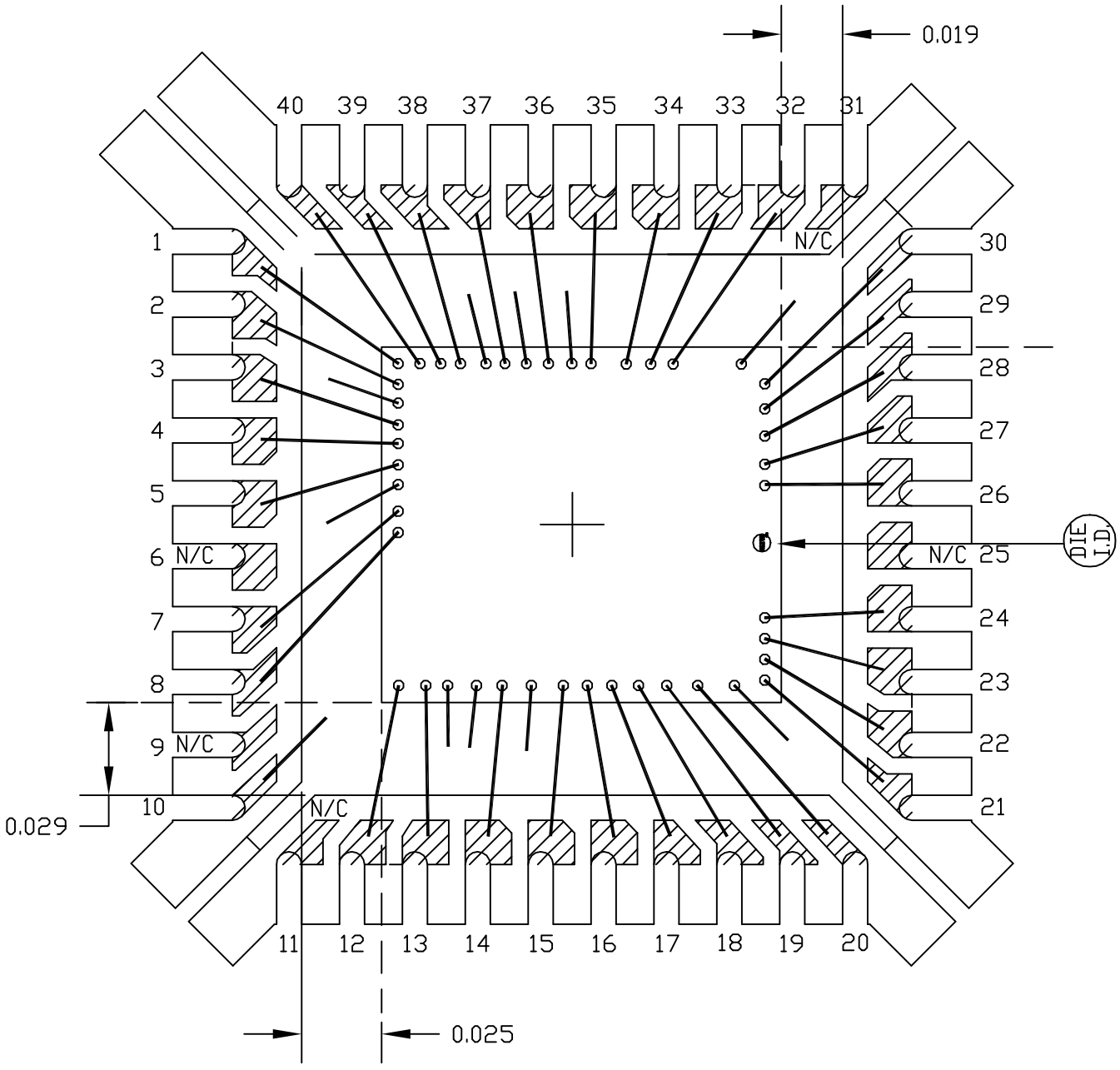
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8

EXPOSED PAD PKG.

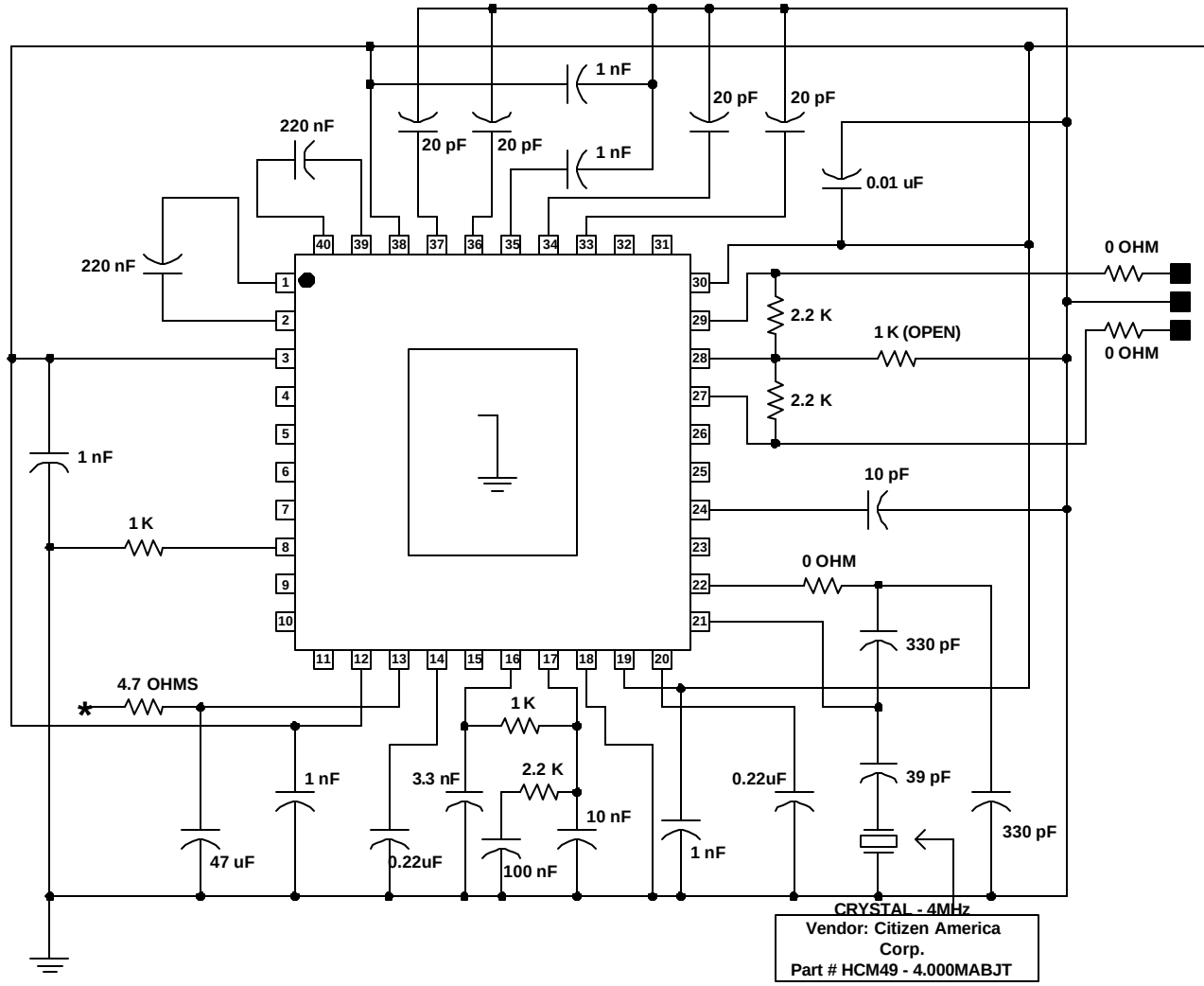


BONDABLE AREA

PKG. BODY SIZE: 6x6 mm

PKG. CODE: G4066-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 169x169	PKG.			BOND DIAGRAM #: 05-7001-0588	REV: A
	DESIGN				

ONCE PER SOCKET



ONCE PER BOARD

+5.25V

100 mil on center holes. (in case we need to populate with ribbon cable connector).

DEVICES: MAX 2116/8
PACKAGE: 40-QFN
MAX. EXPECTED CURRENT = 300mA

DRAWN BY: HAK/TEK TAN

NOTES: Place close to dut those components for pins 3, 12, 13, 16, 17, 19, 20, 21, 22, 30, 35. * Tied to edge finger #24.