RELIABILITY REPORT

FOR

MAX2092ETP+

PLASTIC ENCAPSULATED DEVICES

July 31, 2012

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

| **Approved by** |
|---|
| Richard Aburano |
| Quality Assurance |
| Manager, Reliability Engineering |

**Conclusion**

The MAX2092ETP+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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**I. Device Description**

A. General

The MAX2092 high-linearity analog variable-gain amplifier (VGA) is a monolithic SiGe BiCMOS attenuator/amplifier/error amplifier with an alarm circuit designed to interface with 50  systems operating in the 700MHz to 2700MHz frequency range. The device features a gain range of 18.1dB to -22.3dB, a noise figure of 5.2dB, OIP3 linearity of +32.5dBm, and a wide RF bandwidth. Each of these features makes the device an ideal VGA for numerous receiver and transmitter applications. When paired with the MAX2091 or MAX2091B variable gain upconverter, a complete 2-chip IF-RF signal conditioning solution is possible for microwave point-to-point transmitters.  The MAX2092 operates from a single +5V supply, and is available in a compact 20-pin TQFN package (5mm x 5mm) with an exposed pad. Electrical performance is guaranteed over the extended temperature range from T C = -40°C to +95°C.

## II. Manufacturing Information

| | |
|---|---|
| A. Description/Function: | 700MHz to 2700MHz Analog VGA with Threshold Alarm Circuit and Error Amplifier for Level Control |
| B. Process: | MB3 |
| C. Number of Device Transistors: | 8462 |
| D. Fabrication Location: | USA |
| E. Assembly Location: | China, Taiwan and Thailand |
| F. Date of Initial Production: | June 29. 2012 |

## III. Packaging Information

| | |
|---|---|
| A. Package Type: | 20-pin TQFN 5x5 |
| B. Lead Frame: | Copper |
| C. Lead Finish: | 100% matte Tin |
| D. Die Attach: | Conductive |
| E. Bondwire: | Au (0.8 mil dia.) |
| F. Mold Material: | Epoxy with silica filler |
| G. Assembly Diagram: | #05-9000-4249 |
| H. Flammability Rating: | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C | Level 1 |
| J. Single Layer Theta Ja: | 48°C/W |
| K. Single Layer Theta Jc: | 2°C/W |
| L. Multi Layer Theta Ja: | 32°C/W |
| M. Multi Layer Theta Jc: | 3°C/W |

## IV. Die Information

| | |
|---|---|
| A. Dimensions: | 90.9449X90.9449 mils |
| B. Passivation: | BCB |
| C. Interconnect: | Al with top layer 100% Cu |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | 0.23 microns as drawn |
| F. Minimum Metal Spacing: | 0.23 microns as drawn |
| G. Bondpad Dimensions: | |
| H. Isolation Dielectric: | $SiO_2$ |
| I. Die Separation Method: | Wafer Saw |

## V. Quality Assurance Information

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|---|---|
| A. Quality Assurance Contacts: | Richard Aburano (Manager, Reliability Engineering)<br>Don Lipps (Manager, Reliability Engineering)<br>Bryan Preeshl (Vice President of QA) |
| B. Outgoing Inspection Level: | 0.1% for all electrical parameters guaranteed by the Datasheet.<br>0.1% For all Visual Defects. |
| C. Observed Outgoing Defect Rate: | < 50 ppm |
| D. Sampling Plan: | Mil-Std-105D |

## VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 112C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( $\lambda$) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 1119 \times 78 \times 2}$$ (Chi square value for MTTF upper limit)

(where 1119 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 54.7 \times 10^{-9}$

$\lambda$ = 54.7 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the MB3 Process results in a FIT Rate of 0.08 @ 25C and 1.33 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot SAGG7Q002A, D/C 1217)

The CR55 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.

**Table 1**
Reliability Evaluation Test Results

**MAX2092ETP+**

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | SAMPLE SIZE | NUMBER OF FAILURES | COMMENTS |
|---|---|---|---|---|---|
| **Static Life Test** (Note 1) | | | | | |
| | Ta = 112C<br>Biased<br>Time = 192 hrs. | DC Parameters & functionality | 78 | 0 | SAGG7Q002A, D/C 1217 |

Note 1: Life Test Data may represent plastic DIP qualification lots.