RELIABILITY REPORT

FOR

MAX2090ETP+

PLASTIC ENCAPSULATED DEVICES

January 29, 2013

**MAXIM INTEGRATED**

160 RIO ROBLES

SAN JOSE, CA 95134

| Approved by |
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| Sokhom Chum |
| Quality Assurance |
| Reliability Engineer |

**Conclusion**

The MAX2090ETP+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

**Table of Contents**

**I. .....Device Description**
**II. .....Manufacturing Information**
**III. .....Packaging Information**
**.....Attachments**
**IV. .....Die Information**
**V. .....Quality Assurance Information**
**VI. .....Reliability Evaluation**

**I. Device Description**

A. General

The MAX2090 high-linearity analog variable-gain amplifier (VGA) is a monolithic SiGe BiCMOS attenuator, amplifier, error amplifier, and alarm circuit, designed to interface with 50  systems operating in the 50MHz to 1000MHz frequency range. An external analog control voltage controls the analog attenuator. The device features a gain range of -10.9dB to +26.1dB, a noise figure of 4dB, OIP3 linearity of +38dBm, and a wide RF bandwidth. Each of these features makes the device an ideal VGA for numerous receiver and transmitter applications.  This device operates from a single +5V supply and is available in a compact 20-pin TQFN package (5mm x 5mm) with an exposed pad. Electrical performance is guaranteed over the extended temperature range, from TC = -40°C to +95°C.

## II. Manufacturing Information

| | |
|---|---|
| A. Description/Function: | 50MHz to 1000MHz Analog VGA with Threshold Alarm Circuit and Error Amplifier for Level Control |
| B. Process: | MB3 |
| C. Number of Device Transistors: | 10406 |
| D. Fabrication Location: | California |
| E. Assembly Location: | Taiwan, Thailand |
| F. Date of Initial Production: | September 23. 2011 |

## III. Packaging Information

| | |
|---|---|
| A. Package Type: | 20-pin TQFN 5x5 |
| B. Lead Frame: | Copper |
| C. Lead Finish: | 100% matte Tin |
| D. Die Attach: | Conductive |
| E. Bondwire: | Au (0.8 mil dia.) |
| F. Mold Material: | Epoxy with silica filler |
| G. Assembly Diagram: | #05-9000-4185 |
| H. Flammability Rating: | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C | Level 1 |
| J. Single Layer Theta Ja: | 47°C/W |
| K. Single Layer Theta Jc: | 1.7°C/W |
| L. Multi Layer Theta Ja: | 29°C/W |
| M. Multi Layer Theta Jc: | 1.7°C/W |

## IV. Die Information

| | |
|---|---|
| A. Dimensions: | 116.14 X 104.33 mils |
| B. Passivation: | BCB |
| C. Interconnect: | Al with top layer 100% Cu |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | 0.35um |
| F. Minimum Metal Spacing: | 0.35um |
| G. Bondpad Dimensions: | |
| H. Isolation Dielectric: | $SiO_2$ |
| I. Die Separation Method: | Wafer Saw |

## V. Quality Assurance Information

| | |
|---|---|
| A. Quality Assurance Contacts: | Richard Aburano (Manager, Reliability Engineering)<br>Don Lipps (Manager, Reliability Engineering)<br>Bryan Preeshl (Vice President of QA) |
| B. Outgoing Inspection Level: | 0.1% for all electrical parameters guaranteed by the Datasheet.<br>0.1% For all Visual Defects. |
| C. Observed Outgoing Defect Rate: | < 50 ppm |
| D. Sampling Plan: | Mil-Std-105D |

## VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135¿C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ($\lambda$) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

$\lambda = 22.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the MB3 Process results in a FIT Rate of 0.08 @ 25C and 1.33 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot SL8ZEQ002B D/C 1122)

The CR54 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

**Table 1**
Reliability Evaluation Test Results

**MAX2090ETP+**

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | SAMPLE SIZE | NUMBER OF FAILURES | COMMENTS |
|---|---|---|---|---|---|
| **Static Life Test** (Note 1) | Ta = 135°C<br>Biased<br>Time = 192 hrs. | DC Parameters & functionality | 48 | 0 | SL8ZEQ002E, D/C 1122 |

Note 1: Life Test Data may represent plastic DIP qualification lots.