

RELIABILITY REPORT

FOR

MAX2079CXE+

PLASTIC ENCAPSULATED DEVICES

February 27, 2012

# **MAXIM INTEGRATED PRODUCTS**

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#### Conclusion

The MAX2079CXE+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX2079 fully integrated octal ultrasound receiver is optimized for high channel count, high-performance portable and cart-based ultrasound systems. The easy-to-use integrated receiver allows the user to achieve high-end 2D and Doppler imaging capability using substantially less space and power. The highly compact low-noise amplifier (LNA), variable-gain amplifier (VGA), anti-alias filter (AAF), analog-to-digital converter (ADC), and digital highpass filter (HPF) achieve an ultra-low 2.8dB noise figure at RS = RIN = 200 with a very low 120mW per channel power dissipation at 50Msps. The full receive channel has been optimized for second-harmonic imaging with an exceptional 76dBFS SNR over a 2MHz bandwidth, and -70dBc second-harmonic distortion at fRF = 5MHz over the full receiver gain range. Near-carrier dynamic range has also been optimized for exceptional pulsed and color-flow Doppler performance under high-clutter conditions. The bipolar front-end and CMOS ADC achieve an exceptional near-carrier SNR of 137dBFS/Hz at 1kHz from a 5MHz tone for excellent low-velocity Doppler sensitivity. The device also includes an octal CWD beamformer for a full Doppler solution. Separate mixers for each channel are available for optimal CWD sensitivity. The MAX2079 octal ultrasound front-end is available in a small, 10mm × 10mm, CTBGA package and is specified over the 0°C to +70°C temperature range.



#### II. Manufacturing Information

A. Description/Function: Low-Power, High-Performance, Fully Integrated Octal Ultrasound Receiver

(Octal LNA, VGA, AAF, ADC, and CWD Beamformer)

B. Process: TS18 / CB40

C. Number of Device Transistors:

D. Fabrication Location: Taiwan/USA
E. Assembly Location: Taiwan

F. Date of Initial Production: December 1, 2011

#### III. Packaging Information

A. Package Type: 144-ball CTBGA 10x10

B. Lead Frame: N/AC. Lead Finish: N/A

D. Die Attach: Non-conductive
E. Bondwire: Au (0.8 mil dia.)
F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: #31-4868H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per

JEDEC standard J-STD-020-C

J. Single Layer Theta Ja: °C/W

K. Single Layer Theta Jc: °C/W

L. Multi Layer Theta Ja: 24.7°C/W

M. Multi Layer Theta Jc: 12°C/W

## IV. Die Information

A. Dimensions: 141x299 mils 178x339 mils

B. Passivation: Si<sub>3</sub>N<sub>4</sub>/SiO<sub>2</sub> (Silicon nitride/Silicon dioxide) / Si<sub>3</sub>N<sub>4</sub> (Silicon nitride)

Level 3

C. Interconnect: Al/0.5%Cu / Au

D. Backside Metallization: None

E. Minimum Metal Width: Metal1 = 0.23 / Metal2-3 = 0.28 / Metal4 = 0.44 microns (as drawn) /

Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)

F. Minimum Metal Spacing: Metal1 = 0.23 / Metal2-3 = 0.28 / Metal4 = 0.46 microns (as drawn) /

Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)

G. Bondpad Dimensions:

H. Isolation Dielectric: SiO<sub>2</sub>
 I. Die Separation Method: Wafer saw



#### V. Quality Assurance Information

A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)

Don Lipps (Manager, Reliability Engineering)

Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm</li>D. Sampling Plan: Mil-Std-105D

# VI. Reliability Evaluation

#### A. Accelerated Life Test

The results of the biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( 3) is calculated as follows:

$$\lambda = 1$$
 = 1.83 (Chi square value for MTTF upper limit)   
 $192 \times 4340 \times 130 \times 2$ 

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 14.9 \times 10^{-9}$$
  
 $\lambda = 14.9 \text{ F.I.T. (60% confidence level @ 25°C)}$ 

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the TS18 / CB40 Process results in a FIT Rate of 0.17 / 0.43 @ 25C and 2.94 / 7.33 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot BHDXAAO, D/C 1121)

The CR51 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 1500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.



# **Table 1**Reliability Evaluation Test Results

#### MAX2079CXE+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (	Note 1)				
	Tj = 150C	DC Parameters	45	0	BHDXAAD, D/C 1050
	Biased	& functionality	43	0	BHDXAAJ, D/C 1051
	Time = 192 hrs.		42	0	BHDXAAI, D/C 1051

Note 1: Life Test Data may represent plastic DIP qualification lots.