RELIABILITY REPORT

FOR

MAX2067ETL+

PLASTIC ENCAPSULATED DEVICES

December 15, 2008

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
Director, Reliability Engineering

Conclusion

The MAX2067ETL+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

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I. Device Description

A. General

The MAX2067 high-linearity analog variable-gain amplifier (VGA) is a monolithic SiGe BiCMOS attenuator and amplifier designed to interface with 50Ω systems operating in the 50MHz to 1000MHz frequency range (see the *Typical Application Circuit* in the full data sheet). The analog attenuator is controlled using an external voltage or through the SPI™-compatible interface using an on-chip 8-bit DAC.

Because each stage has its own RF input and RF output, this component can be configured to either optimize NF (amplifier configured first), or OIP3 (amplifier last). The device's performance features include 22dB amplifier gain (amplifier only), 4dB NF at maximum gain (includes attenuator insertion loss), and a high OIP3 level of +43dBm. Each of these features makes the MAX2067 an ideal VGA for numerous receiver and transmitter applications.

In addition, the MAX2067 operates from a single +5V supply with full performance, or a single +3.3V supply with slightly reduced performance, and has an adjustable bias to trade current consumption for linearity performance. This device is available in a compact 40-pin thin QFN package (6mm x 6mm) with an exposed pad. Electrical performance is guaranteed over the extended temperature range (T_C = -40°C to +85°C).

II. Manufacturing Information

A. Description/Function:	50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA
B. Process:	G4
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	ASAT China, UTL Thailand
F. Date of Initial Production:	4/26/2008

III. Packaging Information

A. Package Type:	40-pin TQFN 6x6
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-2877
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	38°C/W
K. Single Layer Theta Jc:	1.4°C/W
L. Multi Layer Theta Ja:	27°C/W
M. Multi Layer Theta Jc:	1.4°C/W

IV. Die Information

A. Dimensions:	122 X 122 mils
B. Passivation:	Si_3N_4
C. Interconnect:	Au
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn) Metal 1, 2 & 3 5.6 microns (as drawn) Metal 4
F. Minimum Metal Spacing:	1.6 microns (as drawn) Metal 1, 2 & 3, 4.2 microns (as drawn) Metal 4
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are complete. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 50 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 21.5 \times 10^{-9}$

λ = 21.5 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the G4 Process results in a FIT Rate of 0.2 @ 25C and 3.6 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The CR42 die type has been found to have all pins able to withstand a HBM transient pulse of +/-500 V per JEDEC JESD22-A114-D. Latch-Up testing has shown that this device withstands a current of +/-250 mA.

Table 1
Reliability Evaluation Test Results

MAX2067ETL+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = dd Biased Time = 192 hrs.	DC Parameters & functionality	50	0
Moisture Testing (Note 2)				
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data