RELIABILITY REPORT

FOR

MAX20317EWP+T

WAFER LEVEL DEVICES

August 23, 2017

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

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Conclusion

The MAX20317EWP+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX20317 is an I^2C controllable, universal 3.5mmØ accessory management IC. The device provides a universal jack interface solution, as well as a compact solution for the power management and interface control of a powered accessory, such as an active noise cancelling (ANC) headset. The MAX20317 automatically measures headset impedance with a high precision, triple current source 8-bit ADC. After impedance detection, the device also detects when a headset is in a CTIA or OMTP configuration and automatically configures the SLEEVE and RING2 terminals to correctly connect the microphone and ground lines. When a boost supply is applied, the MAX20317 can detect the presence of an ANC headset. When the ANC headset is detected and enabled, a button-press monitoring circuit activates, and flags button presses by detecting the voltage drop across a sense resistor. The MAX20317 provides a power line communication tool to a headset to exchange the data with the host device. The MAX20317 has the two separate ground sense inputs from the SLEEVE and RING2 terminals of the connector to provide a high ground isolation to the audio codec. The MAX20317 is available in a space-saving, 20-bump, 0.4mm pitch, 1.65mm x 2.05mm wafer-level package (WLP) and operates over the -40°C to +85°C extended temperature range.

II. Manufacturing Information

A. Description/Function:	Universal 3.5mmØ Accessory Management IC
B. Process:	S18
C. Number of Device Transistors:	72622
D. Fabrication Location:	USA
E. Assembly Location:	Taiwan
F. Date of Initial Production:	May 18, 2017

III. Packaging Information

A. Package Type:	20-bump WLP
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Bondwire:	N/A (N/A mil dia.)
E. Assembly Diagram:	#05-100479
F. Flammability Rating:	Class UL94-V0
G. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
H. Single Layer Theta Ja:	N/A°C/W
I. Single Layer Theta Jc:	N/A°C/W
J. Multi Layer Theta Ja:	55.49°C/W
K. Multi Layer Theta Jc:	N/A°C/W

IV. Die Information

A. Dimensions:	80.7086X64.9606 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Minimum Metal Width:	0.23 microns (as drawn)
E. Minimum Metal Spacing:	0.23 microns (as drawn)
F. Isolation Dielectric:	SiO_2
G. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Eric Wright (Reliability Engineering) Brian Standley (Manager, Reliability) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

$\lambda = 13.7$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.40 @ 25C and 6.96 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The AO05-0 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX20317EWP+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.