RELIABILITY REPORT

FOR

**MAX202ExxE**

PLASTIC ENCAPSULATED DEVICES

February 22, 2002

**MAXIM INTEGRATED PRODUCTS**

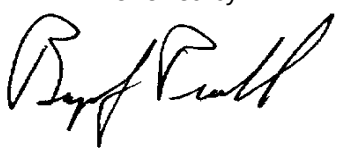
120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

Jim Pedicord
Quality Assurance
Reliability Lab Manager

Reviewed by



Bryan J. Preeshl
Quality Assurance
Executive Director

## Conclusion

The MAX202E successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

## Table of Contents



## I. Device Description

### A. General

The MAX202E line driver/receiver is designed for RS-232 and V.28 communications in harsh environments. Each transmitter output and receiver input is protected against ±15kV electrostatic discharge (ESD) shocks, without latchup. The driver and receiver for the device meets all EIA/TIA-232E and CCITT V.28 specifications at data rates up to 120kbps, when loaded in accordance with the EIA/TIA-232E specification.

The MAX202E comes in 16-pin narrow SO, wide SO, and DIP packages. The MAX202E operates with four 0.1µF capacitors, further reducing cost and board space.

### B. Absolute Maximum Ratings

| Item | Rating |
|---|---|
| $V_{CC}$ | -0.3V to +6V |
| V+ | ($V_{CC}$ - 0.3V) to +14V |
| V- | -14V to +0.3V |
| Input Voltages | |
| T_IN | -0.3V to (V+ +0.3V) |
| R_IN | ±30V |
| Output Voltages | |
| T_OUT | (V- -0.3V) to (V+ +0.3V) |
| R_OUT | -0.3V to ($V_{CC}$ + 0.3V) |
| Short Circuit Duration, T_OUT | Continuous |
| Storage Temp. | -65°C to +165°C |
| Lead Temp. (10 sec.) | +300°C |
| Continuous Power Dissipation (TA = +70°C) | |
| 16-Pin PDIP | 842mW |
| 16-Pin NSO | 696mW |
| 16-Pin TSSOP | 755mW |
| 16-Pin WSO | 762mW |
| Derates above +70°C | |
| 16-Pin PDIP | 10.53mW/°C |
| 16-Pin NSO | 8.70mW/°C |
| 16-Pin TSSOP | 9.40mW/°C |
| 16-Pin WSO | 9.52mW/°C |

## II. Manufacturing Information

| | |
|---|---|
| A. Description/Function: | ±15kV ESD-Protected, +5V RS-232 Transceiver |
| B. Process: | MG2 (5 micron metal gate CMOS) |
| C. Number of Device Transistors: | 123 |
| D. Fabrication Location: | California or Oregon, USA |
| E. Assembly Location: | Philippines, Malaysia, or Thailand |
| F. Date of Initial Production: | April, 1996 |

## III. Packaging Information

| A. Package Type: | **16-Lead DIP** | **16-Lead NSO** | **16-Lead TSSOP** | **16-Lead WSO** |
|---|---|---|---|---|
| B. Lead Frame: | Copper | Copper | Copper | Copper |
| C. Lead Finish: | Solder Plate | Solder Plate | Solder Plate | Solder Plate |
| D. Die Attach: | Silver-filled Epoxy | Silver-filled Epoxy | Silver-filled Epoxy | Silver-filled Epoxy |
| E. Bondwire: | Gold (1.3 mil dia.) | Gold (1.3 mil dia.) | Gold (1.3 mil dia.) | Gold(1.3mil dia.) |
| F. Mold Material: | Epoxy with silica filler | Epoxy with silica filler | Epoxy with silica filler | Epoxy w/ silica filler |
| G. Assembly Diagram: | # 05-1901-0063 | # 05-1901-0064 | # 05-1901-0216 | # 05-1901-0065 |
| H. Flammability Rating: | Class UL94-V0 | Class UL94-V0 | Class UL94-V0 | Class UL94-V0 |

I. Classification of Moisture Sensitivity Per JEDEC standard JESD22-A112: Level 1

## IV. Die Information

| | |
|---|---|
| A. Dimensions: | 80x117 mils |
| B. Passivation: | $Si_3N_4/SiO_2$ (Silicon nitride/ Silicon dioxide) |
| C. Interconnect: | Aluminum/Si (Si = 1%) |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | 5 microns (as drawn) |
| F. Minimum Metal Spacing: | 5 microns (as drawn) |
| G. Bondpad Dimensions: | 5 mil. Sq. |
| H. Isolation Dielectric: | $SiO_2$ |
| I. Die Separation Method: | Wafer Saw |

## V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord (Reliability Lab Manager
Bryan Preeshl (Executive Director of QA**)**
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 100 ppm

D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{4.04}{192 \times 4389 \times 320 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 7.49 \times 10^{-9}$

$\lambda = 7.49$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-0264) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The RS22-1 die type has been found to have all pins able to withstand a transient pulse of ± 2500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Additionally, the MAX207E has achieved ±15kV ESD protection using both methods 3015 and IEC 801-2 (air-gap discharge) on the I/O pins. Latch-Up testing has shown that this device withstands a current of ±250mA and/or ±20V.

**Table 1**
Reliability Evaluation Test Results

**MAX202ExxE**

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | PACKAGE | SAMPLE SIZE | NUMBER OF FAILURES |
|---|---|---|---|---|---|
| **Static Life Test** (Note 1) | | | | | |
| | Ta = 135°C<br>Biased<br>Time = 192 hrs. | DC Parameters<br>& functionality | | 320 | 1 |
| **Moisture Testing** (Note 2) | | | | | |
| Pressure Pot | Ta = 121°C<br>P = 15 psi.<br>RH= 100%<br>Time = 168hrs. | DC Parameters<br>& functionality | PDIP<br>NSO<br>TSSOP<br>WSO | 77<br>77<br>77 | 0<br>0<br>0 |
| 85/85 | Ta = 85°C<br>RH = 85%<br>Biased<br>Time = 1000hrs. | DC Parameters<br>& functionality | | 77 | 0 |
| **Mechanical Stress** (Note 2) | | | | | |
| Temperature Cycle | -65°C/150°C<br>1000 Cycles<br>Method 1010 | DC Parameters | | 77 | 0 |

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic package/process data

TABLE II. Pin combination to be tested. 1/ 2/

| | Terminal A (Each pin individually connected to terminal A with the other floating) | Terminal B (The common combination of all like-named pins connected to terminal B) |
|---|---|---|
| 1. | All pins except $V_{PS1}$ 3/ | All $V_{PS1}$ pins |
| 2. | All input and output pins | All other input-output pins |

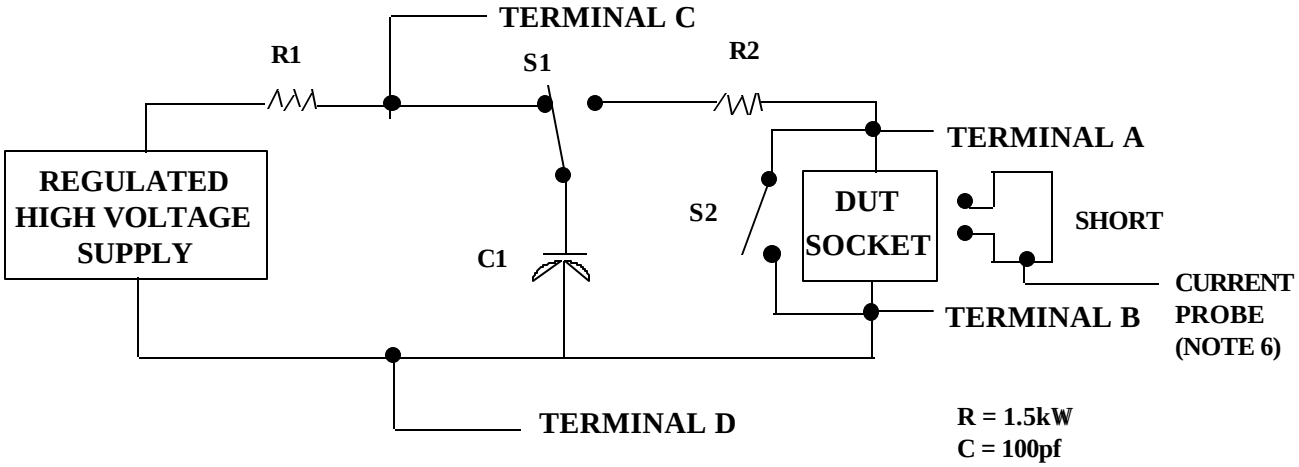
1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where $V_{PS1}$ is $V_{DD}$, $V_{CC}$, $V_{SS}$, $V_{BB}$, GND, $+V_S$, $-V_S$, $V_{REF}$, etc).

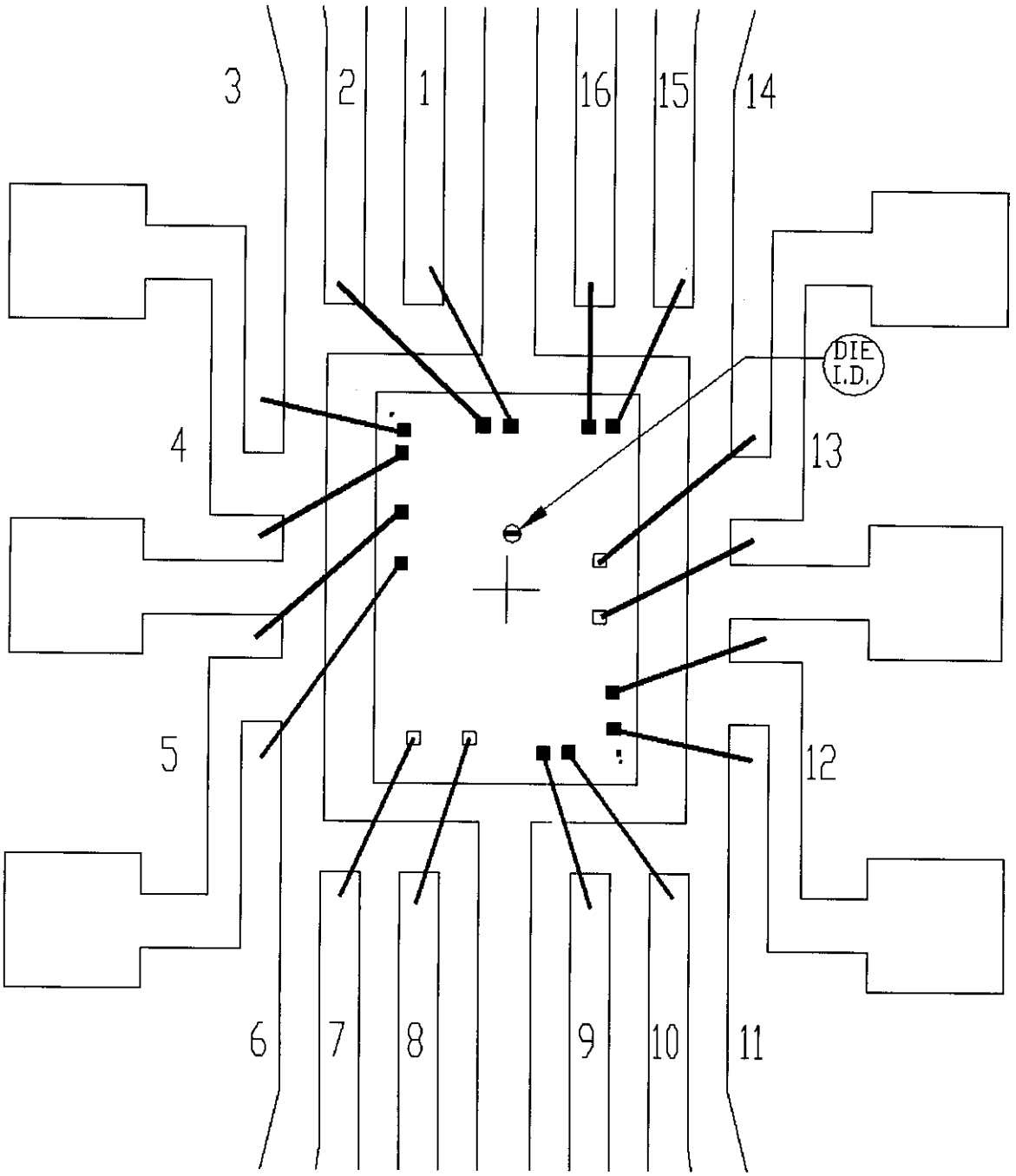
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

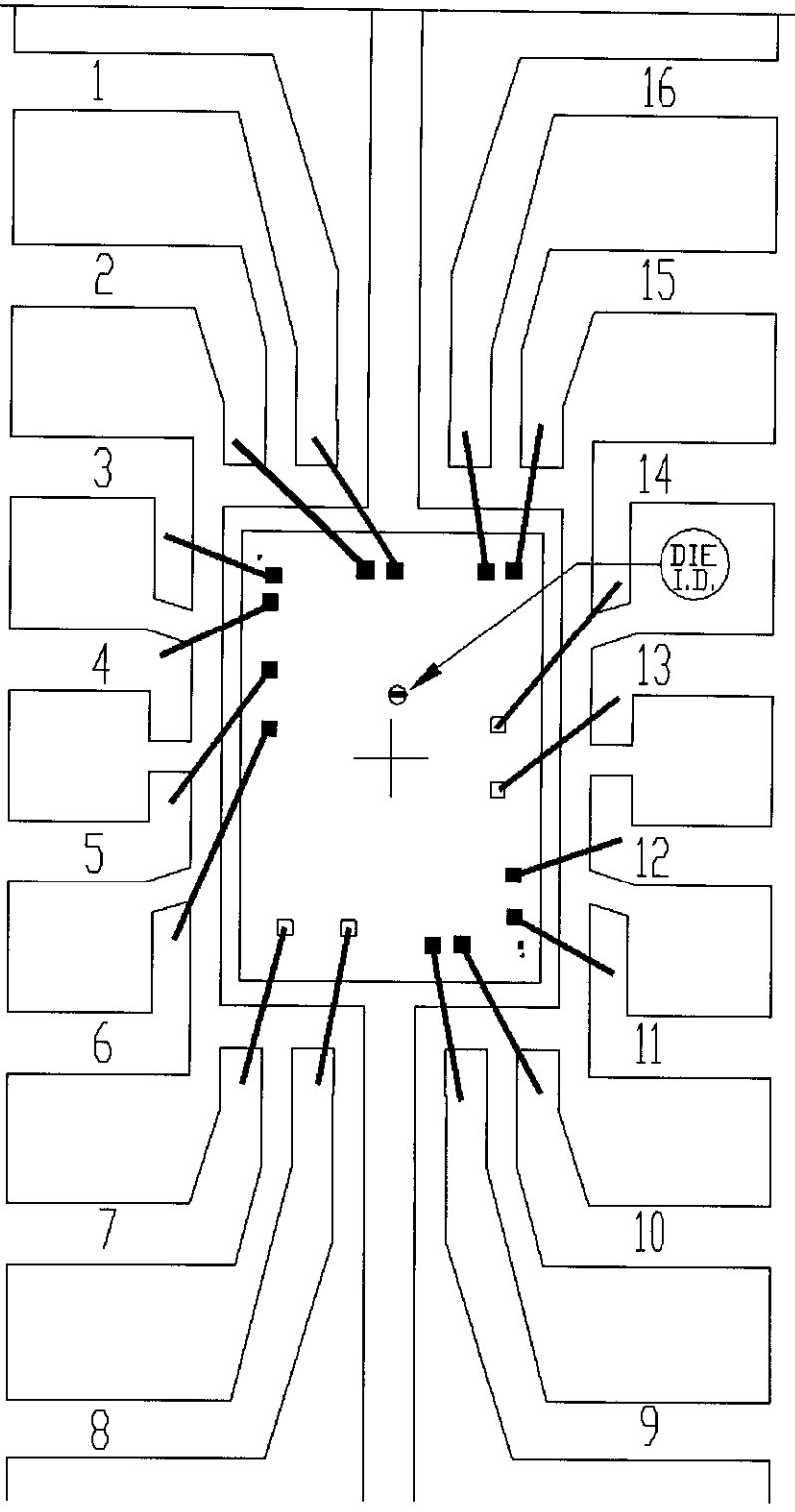
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., $V_{SS1}$, or $V_{SS2}$ or $V_{SS3}$ or $V_{CC1}$, or $V_{CC2}$) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

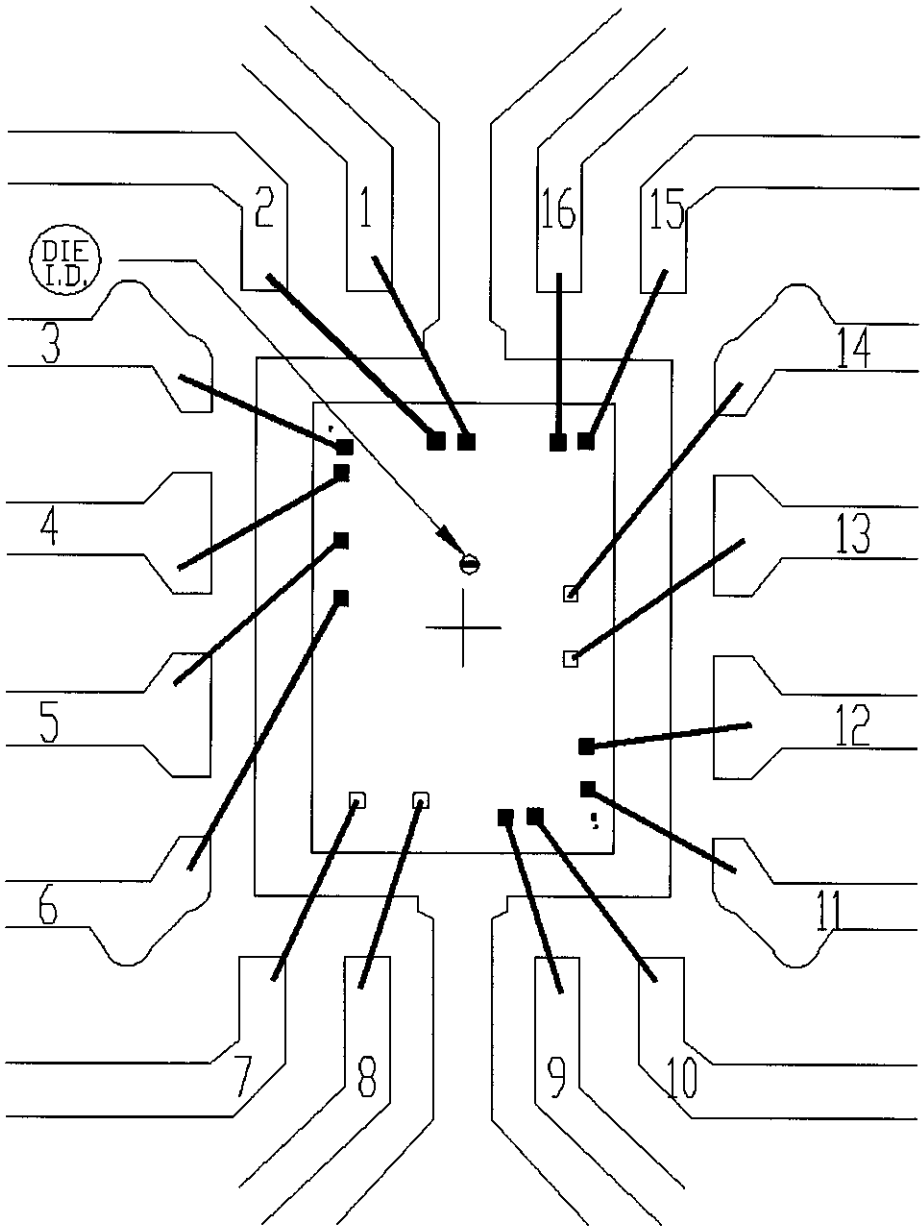




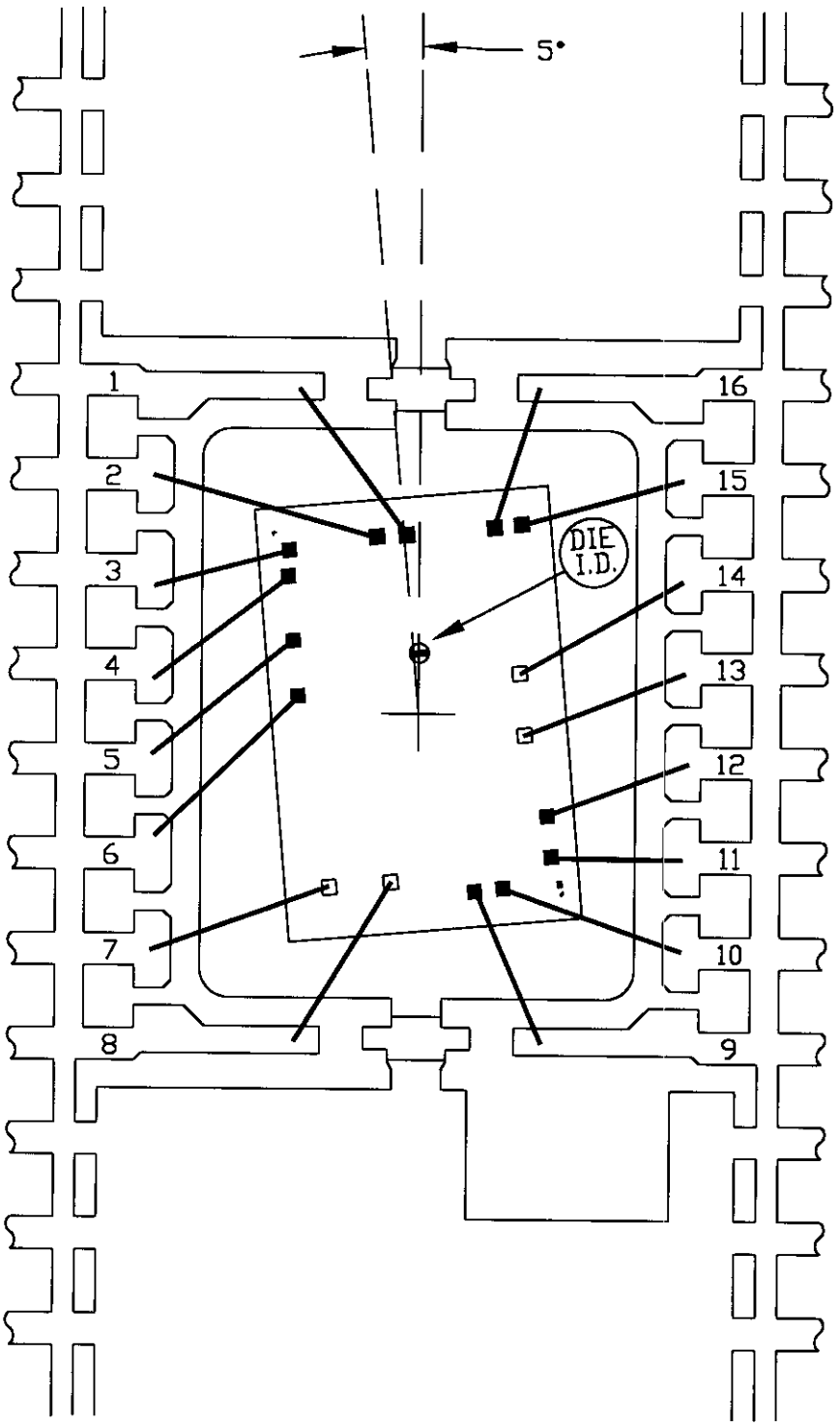

| | | | | |
|---|---|---|---|---|
| PKG.CODE: P16-1 | | APPROVALS | DATE | MAXIM |
| CAV./PAD SIZE: 110 X 140 | PKG. DESIGN | | | BUILDSHEET NUMBER: 05-1901-0063 / REV.: A |



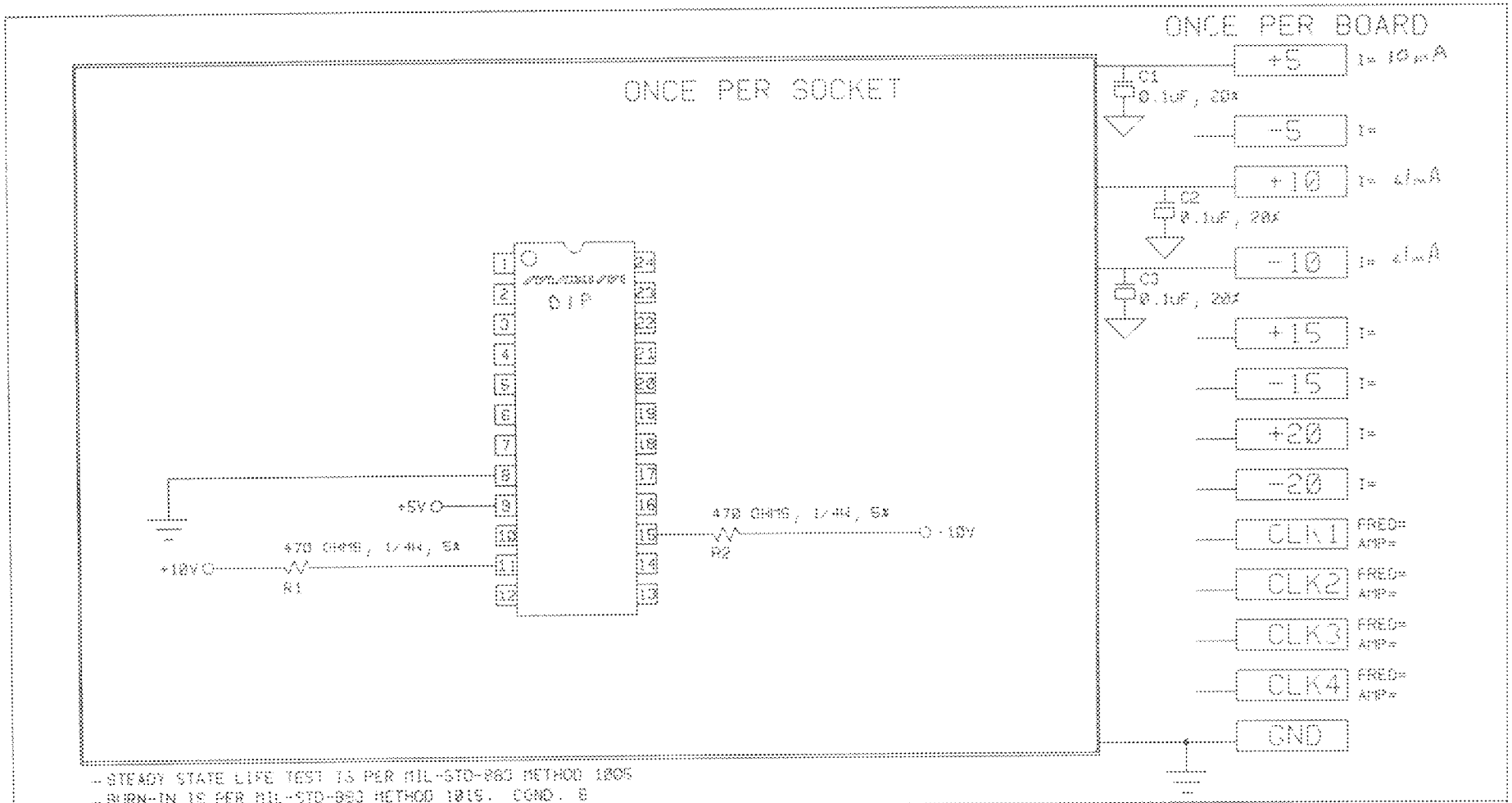

| | | | | |
|---|---|---|---|---|
| PKG.CODE: S16-2 | | APPROVALS | DATE | MAXIM |
| CAV./PAD SIZE: 90 X 130 | PKG. DESIGN | | | BUILDSHEET NUMBER: 05-1901-0064 / REV.: A |




| | | | | |
|---|---|---|---|---|
| PKG.CODE: W16-1 | | APPROVALS | DATE | MAXIM |
| CAV./PAD SIZE: 110 X 140 | PKG. DESIGN | | | BUILDSHEET NUMBER: 05-1901-0065 / REV.: A |




| PKG.CODE: U16-1 | | APPROVALS | DATE | MAXIM |
|---|---|---|---|---|
| CAV./PAD SIZE: 118X154 | PKG. DESIGN | | | BUILDSHEET NUMBER: 05-1901-0216 / REV.: A |




- STEADY STATE LIFE TEST IS PER MIL-STD-883 METHOD 1005
- BURN-IN IS PER MIL-STD-883 METHOD 1015. COND. B

NOTES:

1. TEMPERATURE: 125C OR EQUIVALENT
2. TIME: 160 HOURS MIN. OR EQUIVALENT
3. ALL COMPONENTS AND MATERIAL MUST STAND 150C CONTINUOUS
4. APPROVED FOR [X] COMMERCIAL
   [X] MR/883

SPEC. NO. 06-264 REV. A

DATE: 4/3/92

DRAWN BY:

MAXIM BURN-IN SCHEMATIC

DEVICE TYPE:

MAX237/9/207/208